bq25910 I²C Controlled 6-A Three-Level Switch Mode, Single-Cell Parallel Battery Charger for Fast Charging

1 Features

- Parallel Charger Operation Provides Fast Charging in Dual Charger Configuration
- High Efficiency 750-kHz Switch Mode Three-Level Buck Parallel Charger
  - Reduced Ripple to Support Low Profile Inductor
  - 95.4% Charge Efficiency at 1.5 A from 5-V Input
  - 93.3% Charge Efficiency at 3 A from 9-V Input
  - Superior Efficiency Compared to Traditional Buck Converter in Compact Form Factor
- Single Input to Support USB Input and Adjustable High Voltage Adapters
  - Support 3.9-V to 14-V Input Voltage Range with 20-V Absolute Maximum Input Voltage Rating
  - Input Current Limit (500 mA to 3.6 A with 100-mA resolution) to Support USB2.0 and USB 3.0 Standard and High Voltage Adaptors
  - Maximum Power Tracking by Input Voltage Limit (VINDPM) up to 14 V
- Flexible I²C Mode for Optimal System Performance
- High Integration Includes all MOSFETs, Current Sensing and Loop Compensation
  - Lossless Charge Current Sensing without Sense Resistor
- < 10-µA Low Battery Leakage Current During Stand-By Mode
- High Accuracy
  - ±0.4% Charge Voltage Regulation
  - ±10% Charge Current Regulation
  - ±7.5% Input Current Regulation
  - Remote Differential Battery Sensing
- Safety
  - Thermal Regulation and Thermal Shutdown
  - Input UVLO and Overvoltage Protection
  - Battery OVP
  - Input Dynamic Power Management (DPM)
  - Charging Safety Timer
  - Flying Capacitor Short Circuit Protection
  - Output Voltage Short Circuit Protection
- Available in 36-Ball WCSP Package

2 Applications

- Smart Phone
- Tablet
- Wireless Charging
- Portable Electronics
- Electronic Point of Sales (ePOS)

3 Description

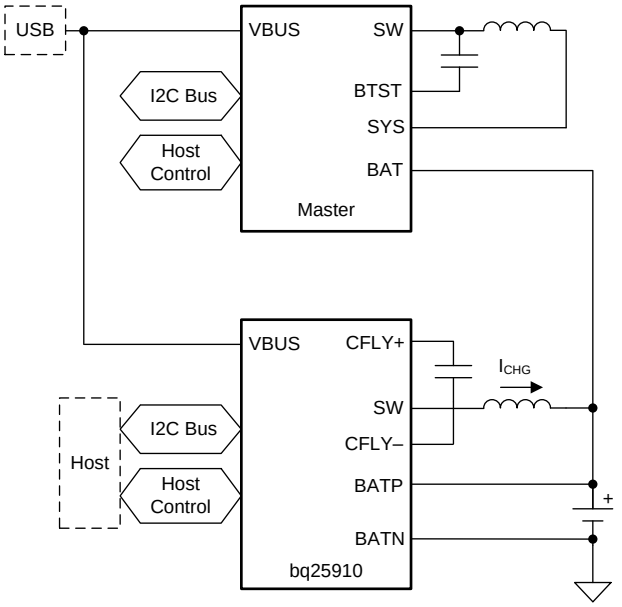
The bq25910 is an integrated three-level switch-mode parallel battery charge management device for single cell Li-ion and Li-polymer batteries. Utilization of the three-level converter maintains highest switch-mode operation efficiency while reducing solution footprint and increasing power density. The device supports fast charging with high input voltage for a wide range of portable devices. The solution integrates reverse-blocking FET (Q_{BLK}), and four switching FETs (Q_{HSA}, Q_{HSB}, Q_{LSB}, Q_{LSA}). The I²C serial interface with charging and system settings makes the device a truly flexible solution.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
bq25910	DSBGA (36)	2.41 mm x 2.44 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Original (September 2017) to Revision A	Page
• Changed from Advance Information to Production Data	1

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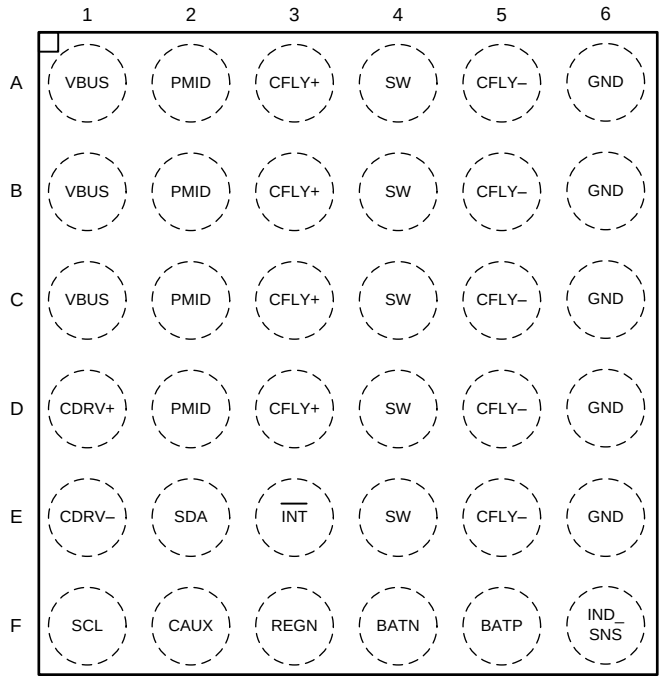
5 Pin Configuration and Functions

bq25910-YFF (I^2C controlled)
36-Pin DSBGA
Top View



(1) Top View = Xray through a soldered down part with A1 starting in upper left hand corner.

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Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BATN	F4	AI	**Negative Battery Sense Terminal –** Kelvin connect via 100-Ω resistor as close as possible to negative battery terminal
BATP	F5	AI	**Positive Battery Sense Terminal –** Kelvin connect via 100-Ω resistor as close as possible to positive battery terminal
CAUX	F2	P	**Auxiliary Capacitor –** Bypass CAUX to GND with at least a 4.7-μF, 10-V ceramic capacitor
CDRV+	D1	P	**Gate Drive Supply Positive Terminal –** CDRV is used to generate multilevel gate drive rails. Connect a 220-nF, 6.3-V ceramic capacitor across CDRV+ and CDRV-.
CDRV–	E1	P	**Gate Drive Supply Negative Terminal –** CDRV is used to generate multilevel gate drive rails. Connect a 220-nF, 6.3-V ceramic capacitor across DRV+ and DRV-.
CFLY+	A3	P	**Flying Capacitor Positive Terminal –** Connect 20-μF, 16-V ceramic capacitor across CFLY+ and CFLY–. Refer to *Application and Implementation* section for more information on selecting CFLY.
	B3		
	C3		
	D3		
CFLY–	A5	P	**Flying Capacitor Negative Terminal –** Connect 20-μF, 16-V ceramic capacitor across CFLY+ and CFLY–. Refer to *Application and Implementation* section for more information on selecting CFLY.
	B5		
	C5		
	D5		
	E5		
GND	A6	-	**Ground Return**
	B6		
	C6		
	D6		
	E6		
IND_SNS	F6	AI	**Output Inductor Sense Input –** Kelvin connect as close as possible to the output of the switched inductor.
$\overline{\text{INT}}$	E3	DO	**Open-Drain Interrupt Output –** Connect $\overline{\text{INT}}$ to the logic rail via a 10-kΩ resistor. The $\overline{\text{INT}}$ pin sends active low, 256-μs pulse to the host to report charger device status and fault.
PMID	A2	P	**Reverse Blocking MOSFET and QHSA MOSFET Connection –** Given the total input capacitance, place 1 μF on VBUS, and the rest on PMID, as close to the device as possible. Typical value: 10-μF, 25-V ceramic capacitor
	B2		
	C2		
	D2		
REGN	F3	P	**Gate Drive Supply –** Bias supply for internal MOSFETs driver and device. Bypass REGN to GND with a 4.7-μF, 10-V ceramic capacitor.
SCL	F1	DI	**I^2C Interface Open-Drain Clock Line –** Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	E2	DIO	**I^2C Interface Open-Drain Data Line –** Connect SDA to the logic rail through a 10-kΩ resistor.
SW	A4	P	**Inductor Connection –** Connect to the switched side of the external inductor (Recommended: 330 nH for up to 9-V applications or 470 nH for up to 12-V applications). Refer to *Application and Implementation* section for more information on selecting inductor.
	B4		
	C4		
	D4		
	E4		
VBUS	A1	P	**Input Supply –** VBUS is connected to the external DC supply. Bypass VBUS to GND with at least 1-μF, 25-V ceramic capacitor, placed as close to the device as possible.
	B1		
	C1		

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
Voltage range (with respect to GND)	VBUS (converter not switching)		–2	20	V
	PMID (converter not switching)		–0.3	20	V
	CDRV+, CDRV-		–0.3	20	V
	CFLY+		–0.3	16(2)	V
	CFLY+ to SW, SW to CFLY–, CFLY– to GND, CAUX to GND	DC	–0.3	7	V
		Pulse < 30ns	–0.3	11	V
	BATP, BATN, IND_SNS		–0.3	6	V
	REGN		–0.3	6	V
Voltage range (with respect to GND)	SDA, SCL, /INT		–0.3	6	V
Output sink current	/INT			6	mA
Junction Temperature, T_J			–40	150	°C
Storage temperature, T_{stg}			–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This condition is contingent on the fact that $0V < V_{CFLY} < 8V$

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±250	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	3.9		14(1)	V
I_{VBUS}	Average input current (VBUS)			3.3	A
I_{SW}	Average output current (SW)			6	A
V_{BAT}	Battery voltage (BATP - BATN)			4.775	V
T_A	Operating free-air temperature	–40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on either CFLY+, SW, or CFLY- pins. A tight layout minimizes switching noise.

6.4 Thermal Information

THERMAL METRIC(1)		bq25910 YFF (DSBGA) 36-PINS	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	52.8	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	0.3	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	11.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	11.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

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6.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BATP, BATN, SW)	VBAT = 4.5V, VBUS = 0 - 5V, SCL, SDA = 0V or 1.8V, T_J < 85°C, EN_CHG = 0		6.5	10	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in HIZ	VBUS = 5V, High-Z Mode, no battery			30	µA
		VBUS < V_{VBUS_OV}, High-Z Mode, no battery			50	µA
I_{VBUS}	Input supply current (VBUS)	VBUS > V_{SLEEPZ}, V_{BAT} = 3.8V, ICHG = 0A, converter not switching			20	µA
		VBUS > V_{SLEEPZ}, V_{BAT} = 3.8V, converter switching, IOUT = 0A		13		mA
VBUS / VBAT POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		14	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising	3.6			V
V_{SLEEP}	Enter sleep mode threshold	VBUS falling, VBUS - VBAT, VBAT = 4V, T_J = 0°C - 85°C	15	60	110	mV
V_{SLEEPZ}	Exit sleep mode threshold	VBUS rising, VBUS - VBAT, VBAT = 4V, T_J = 0°C - 85°C	115	220	275	mV
V_{VBUS_OV}	VBUS over-voltage rising threshold	VBUS rising	14	14.3	14.7	V
	VBUS over-voltage falling threshold	VBUS falling	13.3	13.65	14	V
V_{BAT_UVLOZ}	Battery for active I2C, no VBUS		2.3			V
$V_{POORSRC}$	Bad adapter detection threshold			3.7		V
$I_{POORSRC}$	Bad adapter detection current source			20		mA
POWER-PATH						
R_{ON_QBLK} (QBLK)	Top reverse blocking MOSFET on-resistance between VBUS and PMID (QBLK)	T_J = –40°C - 125°C		14	22	mΩ
R_{ON_QHSA} (Q1)	Outer, high-side switching MOSFET on-resistance between PMID and CFLY+ (Q1)	T_J = –40°C - 125°C		22	40	mΩ
R_{ON_QHSB} (Q3)	Inner, high-side switching MOSFET on-resistance between CFLY+ and SW (Q3)	T_J = –40°C - 125°C		12	20	mΩ
R_{ON_QLSB} (Q4)	Inner, low-side switching MOSFET on-resistance between SW and CFLY- (Q4)	T_J = –40°C - 125°C		8	13	mΩ
R_{ON_QLSA} (Q2)	Outer, low-side switching MOSFET on-resistance between CFLY- and GND (Q2)	T_J = –40°C - 125°C		8	13	mΩ
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.5		4.775	V
V_{REG_STEP}	Typical charge voltage regulation step			5		mV
V_{REG_ACC}	Charge voltage regulation accuracy	VREG = 4.2V or 4.35V or 4.4V, T_J = –40°C - 85°C	-0.4		0.4	%
I_{CHG_RANGE}	Typical charge current regulation range		1000		6000	mA
I_{CHG_STEP}	Typical charge current regulation step			50		mA
I_{CHG_ACC}	Charge current regulation accuracy	ICHG = 2A, 3A, 4A, 5A, 6A, T_J = –40°C - 85°C	-10		10	%

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Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TERM_ACC}	Termination current regulation accuracy	VBUS = 9V, ICHG = 4A, ITERM = 1.0A, T_J = 0°C - 85°C	0.9	1	1.1	A
V_{BAT_SHORT}	Short battery voltage falling threshold	VBAT falling	1.85	2.00	2.15	V
V_{BAT_LOWV}	VBAT LOWV Rising threshold to start fast-charging	VBAT rising, VBATLOW = 3.2V	3.1	3.2	3.3	V
	VBAT LOWV Falling threshold to stop fast-charging	VBAT falling, VBATLOW = 3.2V	2.9	3	3.1	V
V_{BAT_LOWV}	VBAT LOWV Rising threshold to start fast-charging	VBAT rising, VBATLOW = 3.5V	3.4	3.5	3.6	V
	VBAT LOWV Falling threshold to stop fast-charging	VBAT falling, VBATLOW = 3.5V	3.2	3.3	3.4	V
R_{BATP}	BATP Input resistance	VBAT = 4V, VBUS = 5V, EN_CHG = 0		0.6		MΩ
R_{BATN}	BATN Input resistance	VBAT = 4V, VBUS = 5V, EN_CHG = 0		0.6		MΩ
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Input voltage regulation range		3.9		14	V
V_{INDPM_STEP}	Input voltage regulation step			100		mV
V_{INDPM_ACC}	Input voltage regulation accuracy	VINDPM = 4.3V	4.121	4.3	4.447	V
		VINDPM = 7.8V	7.566	7.8	8.034	V
		VINDPM = 10.8V	10.476	10.8	11.124	V
I_{INDPM_RANGE}	Input current regulation range		500		3600	mA
I_{INDPM_STEP}	Input current regulation step			100		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500mA, T_J = –40°C - 85°C	410		500	mA
		IINDPM = 1500mA, T_J = –40°C - 85°C	1275		1500	mA
		IINDPM = 2500mA, T_J = –40°C - 85°C	2125		2500	mA
		IINDPM = 3000mA, T_J = –40°C - 85°C	2540		3000	mA
BATTERY OVER-VOLTAGE PROTECTION						
V_{BAT_OVP}	Battery over-voltage rising threshold	VBAT rising, as percentage of VREG	102	104	106	%
	Battery over-voltage falling threshold	VBAT falling, as percentage of VREG	100	102	103	%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 80°C		80		°C
		TREG = 120°C		120		°C
T_{SHUT}	Thermal Shutdown Rising threshold	Temperature Increasing		150		°C
	Thermal Shutdown Falling threshold	Temperature Decreasing		120		°C
BUCK MODE OPERATION						
F_{SW}	PWM switching frequency	Switching-node frequency	1.35	1.5	1.65	MHz
D_{MAX}	Maximum PWM Duty Cycle			97		%
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 12V, I_{REGN} = 40mA	4.85	5		V
		V_{VBUS} = 5V, I_{REGN} = 20mA	4.7	4.8		V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5V, V_{REGN} = 3.8V	50			mA

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Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = –40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL	Pull-up rail 1.8V	1.3			V
V_{IL}	Input low threshold level, SDA and SCL	Pull-up rail 1.8V			0.4	V
V_{OL}	Output low threshold level, SDA	Sink current = 5mA			0.4	V
I_{BIAS}	High level leakage current, SDA and SCL	Pull-up rail 1.8V			1	µA
LOGIC OUTPUT PIN (/INT)						
V_{OL}	Output low threshold level	Sink current = 5mA			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8V			1	µA

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6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBUS/BAT POWER UP						
t_{VBUS_OV}	VBUS OVP reaction time	VBUS rising above V_{BUS_OV} threshold to converter turn off		200		ns
$t_{POORSRC}$	Bad adapter detection duration			30		ms
BATTERY CHARGER						
$t_{BAT\_LOWV\_DGL}$	Deglitchg time for BAT_LOWV comparator	VBAT crossing VBAT_LOWV threshold (rising and falling)		20		ms
t_{TERM_DGL}	Deglitch time for charge termination	Charge current falling below I_{TERM}		250		ms
t_{BATOVP_DGL}	Deglitch time for battery over-voltage to disable charge			1		µs
t_{SAFETY}	Charge Safety Timer Accuracy	CHG_TIMER[1:0] = 12 hours	10.8	12	13.2	hr
I2C INTERFACE						
f_{SCL}	SCL clock frequency				1000	kHz
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{DIG}	Digital clock	REGN LDO enabled	1.35	1.5	1.65	MHz
t_{WDT}	Watchdog Reset time	WATCHDOG[1:0] = 160s, REGN LDO enabled	136	160		sec

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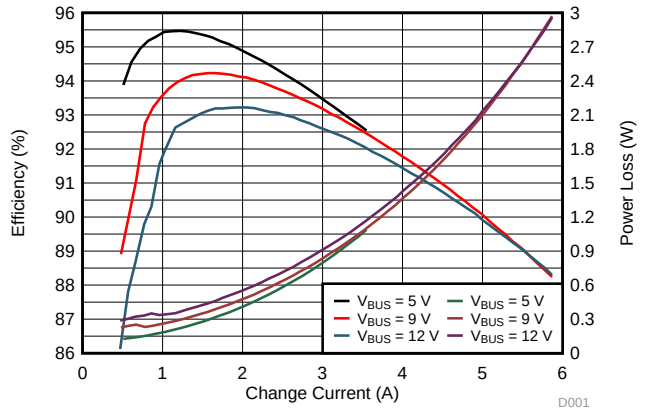
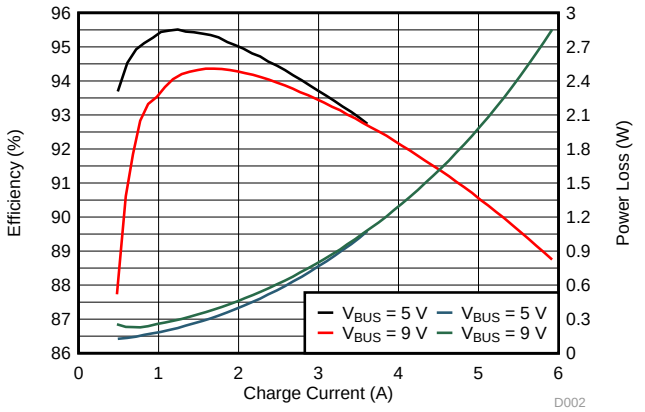
6.7 Typical Characteristics



VBAT = 3.8 V, Inductor = DFE252012F-R47 (470 nH, 23 mΩ max)

Figure 1. Charge Efficiency vs Charge Current



VBAT = 3.8 V, Inductor = HMLQ25201B-R33 (330 nH, 17 mΩ max)

Figure 2. Charge Efficiency vs Charge Current

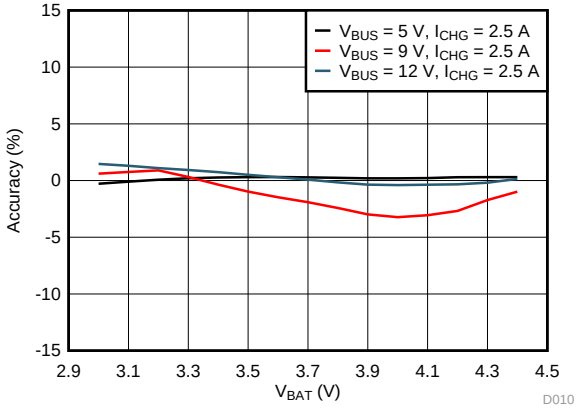
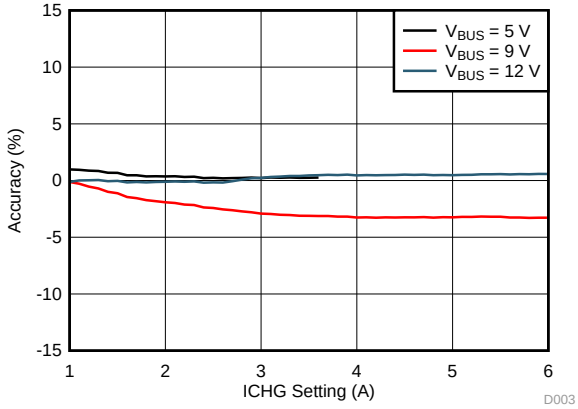
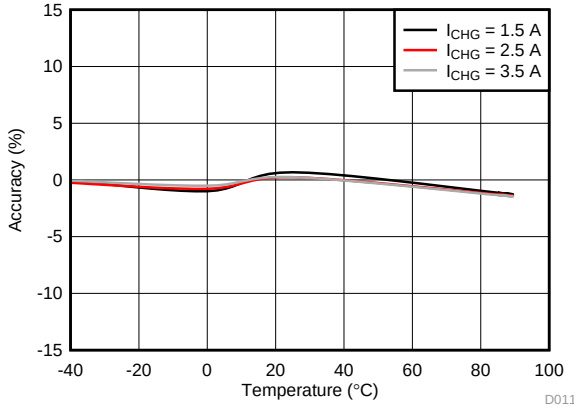


Figure 3. Charge Current Accuracy vs Battery Voltage



VBAT = 3.8 V

Figure 4. Charge Current Accuracy vs I²C ICHG Setting



VBUS = 5 V, VBAT = 3.8 V

Figure 5. Charge Current Accuracy vs Temperature

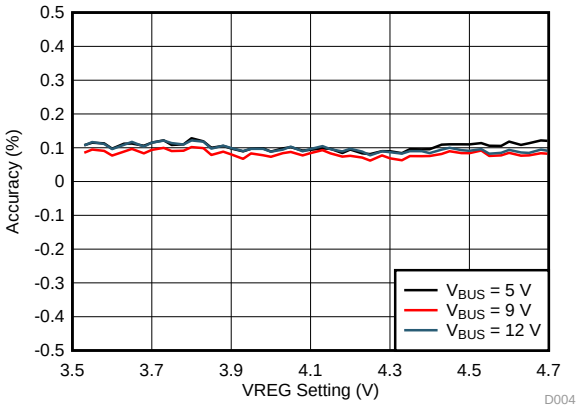
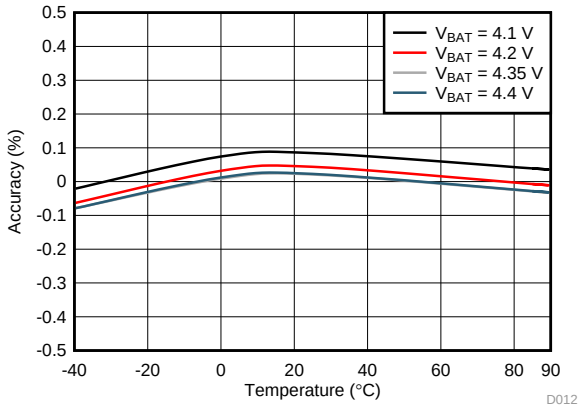


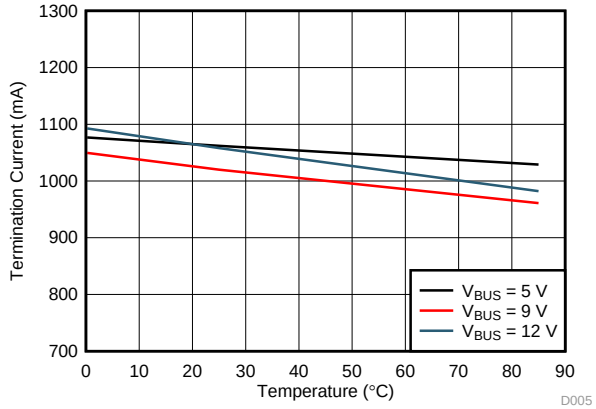
Figure 6. Battery Voltage Regulation Accuracy vs I²C VREG Setting

Typical Characteristics (continued)



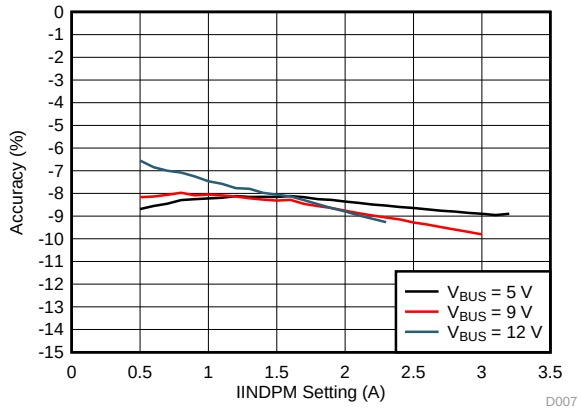
VBUS = 9 V

Figure 7. Battery Voltage Regulation Accuracy vs Temperature



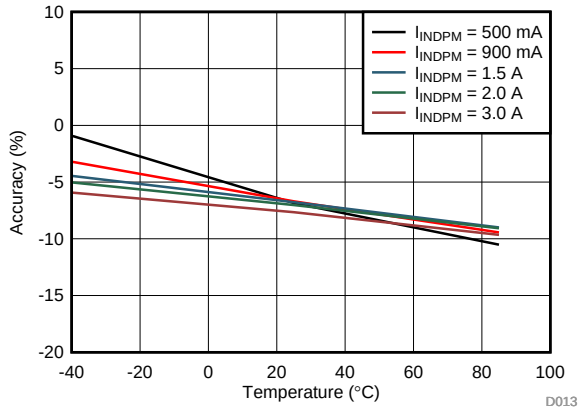
VREG = 4.35 V

Figure 8. Termination Current vs Temperature



VBAT = 3.8 V

Figure 9. Input Current Limit Accuracy vs I²C IINDPM Setting



VBUS = 5 V, VBAT = 3.8 V

Figure 10. Input Current Limit Accuracy vs Temperature

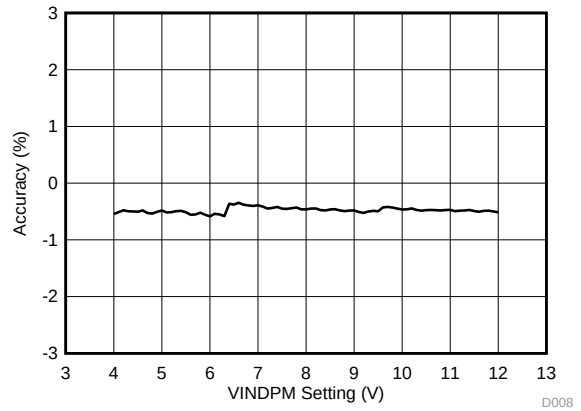
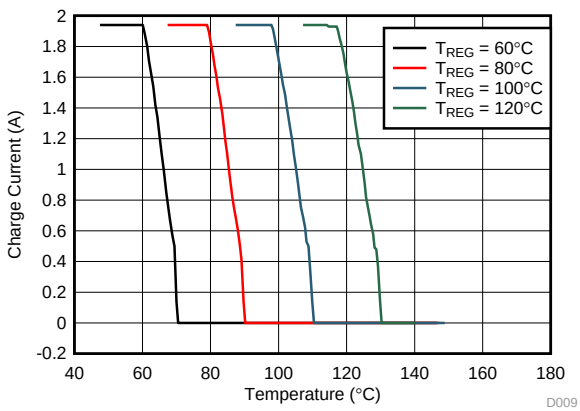


Figure 11. Input Voltage Limit Accuracy vs I²C VINDPM Setting



ICHG = 1.9 A

Figure 12. Charge Current vs Temperature

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7 Detailed Description

7.1 Overview

The bq25910 is an integrated three-level switch-mode parallel battery charge management device for single cell Li-ion and Li-polymer batteries. Utilization of the three-level converter maintains highest switch-mode operation efficiency while reducing solution footprint and increasing power density. The device supports fast charging with high input voltage for a wide range of portable devices. The solution integrates reverse-blocking FET (Q_{BLK}), and four switching FETs (Q_{HSA}, Q_{HSB}, Q_{LSB}, Q_{LSA}). The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, and USB compliant adjustable high voltage adapter. The device is compliant with USB 2.0 and USB 3.0 power specifications with input current and voltage regulation.

After initiating a charging cycle with host control, the device completes a charging cycle without software control. It automatically detects battery voltage and charges the battery in two-phases: constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit (termination current) in the constant voltage phase.

The device provides various safety features for battery charging, including charging safety timer, battery over-voltage, and over-current protections. Thermal regulation reduces charge current when the device junction temperature exceeds 120°C (programmable via I^2C). The $\overline{INT}$ output immediately notifies the host when the charger changes state or a fault occurs.

The bq25910 is available in space-saving 36-bump 2.41 x 2.44 mm^2 WCSP.

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7.2 Functional Block Diagram

The device is a highly integrated 6-A three-level switch-mode parallel battery charger for single-cell Li-ion and Li-polymer batteries. It integrates a reverse-blocking FET (QBLK), four switching FETs for three-level operation (QHSA – QLSA), and bootstrap cap control to drive HS gates.

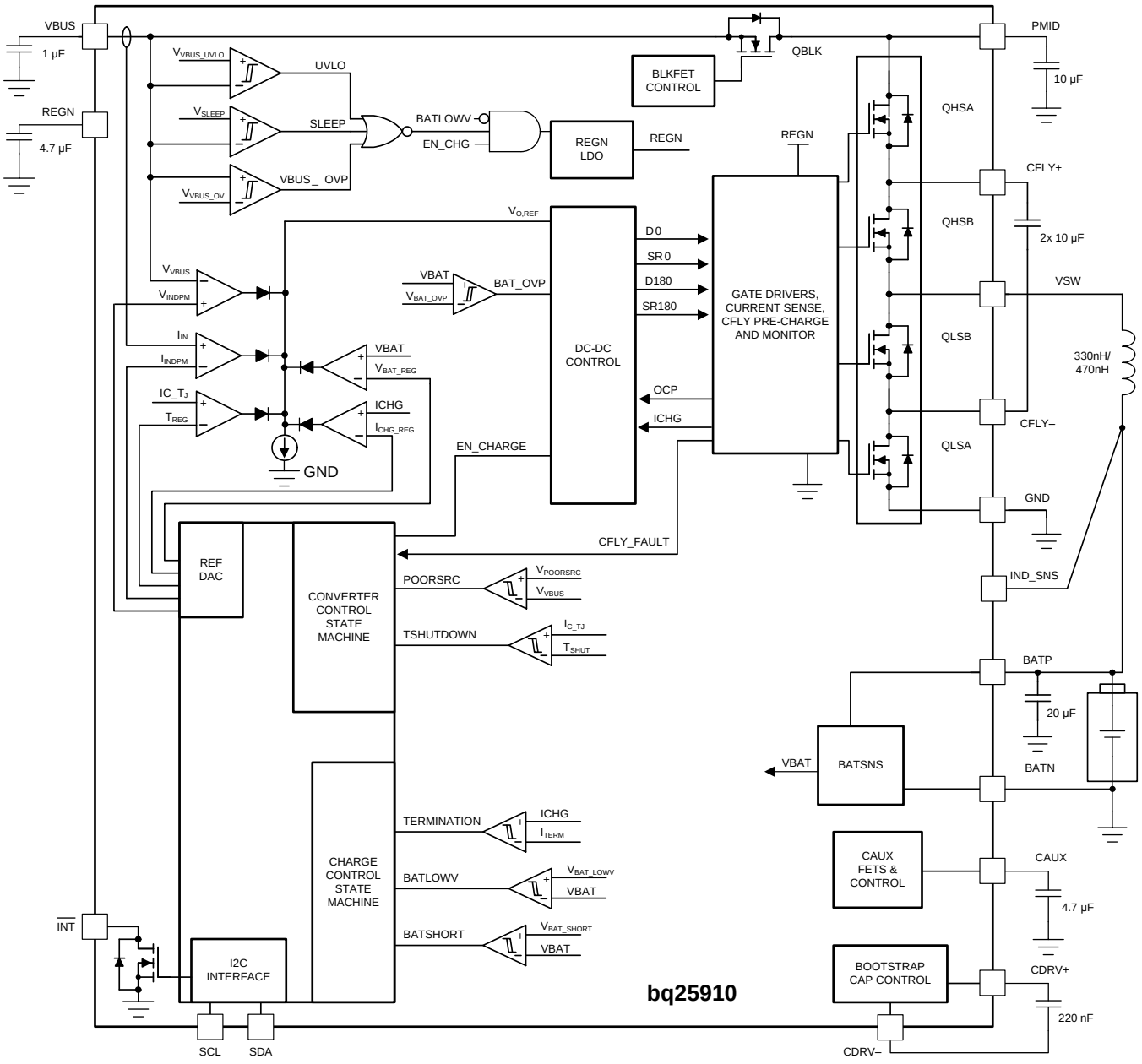

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Figure 13. bq25910 I²C Controlled Functional Block Diagram

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7.3 Feature Description

7.3.1 Device Power-On-Reset (POR)

The internal bias circuits are powered from the higher voltage of VBUS and VBAT. When V_{VBUS} rises above V_{VBUS_UVLOZ}, or V_{BAT} rises above V_{BAT_UVLOZ}, the sleep comparator and battery depletion comparator are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

7.3.2 Device Power Up from Battery without Input Source

If only battery is present, the device consumes up to I_{BAT} quiescent current. The REGN LDO stays off to minimize the current draw. I^2C interface is ready for communication as long as V_{BAT} is above V_{BAT_UVLOZ}.

7.3.3 Device Power Up from Input Source

When an input source is plugged in, and the EN_CHG bit is set to 1, the device checks the input source voltage and battery voltage to turn on REGN LDO, all the bias circuits and begin charging. The startup sequence from input source is as listed:

1. Power up REGN LDO
2. Poor source qualification
3. C_{FLY} and C_{AUX} pre-charging routine
4. Converter Power-up

7.3.4 Power Up REGN LDO

The REGN LDO supplies internal bias circuits and power FET gate drivers. The pull-up rail of $\overline{INT}$ can be connected to REGN as well. The REGN LDO is enabled when all the following conditions are met:

1. VBUS above V_{BUS_UVLOZ}
2. VBUS above V_{BAT} + V_{SLEEPZ}
3. VBUS below V_{VBUS_OV}
4. V_{BAT} above V_{BAT_LOWV}
5. EN_CHG bit = 1
6. ICHG ≠ 0 A

If one of the above conditions is not met, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS in this state.

7.3.5 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to operate the buck converter:

1. VBUS voltage below V_{VBUS_OV}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$ (typical 20 mA)

Once the conditions are met, the status register bit PG_STAT is set high and the $\overline{INT}$ pin is pulsed to signal the host. If VBUS_OV is detected (condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (condition 2 above), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device sets POORSRC_STAT, sends an $\overline{INT}$ pulse to notify the host, goes to HIZ mode and resets EN_CHG bit. Adapter re-plugin and/or EN_CHG toggle is required to restart device operation.

7.3.6 Converter Power-Up

Prior to converter switching, the flying and auxiliary capacitors, CFLY, and CAUX are charged to VBUS/2. After the capacitors have been pre-charged, the converter is enabled and the switching FETs Q_{HSA} – Q_{LSB} start switching. As a battery charger, the device deploys a highly-efficient 750-kHz three-level step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

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Feature Description (continued)

The charge current is soft-started into the desired value by starting from 300 mA and increasing the current up to ICHG programmed value over time. This "soft-start" also applies when increasing the ICHG register value while charging.

7.3.7 Three-Level Buck Converter Theory of Operation

The three-level converter is a combination of a switched capacitor and a switched inductor circuit. Assuming the flying capacitor, CFLY, remains balanced at VIN/2, the VSW node can be presented with three different voltages: VIN, VIN/2, and GND. The gate driving scheme is similar to a two-phase buck converter. The outer FETs (QHSA and QLSA) are driven with a complimentary signal with duty cycle D = VOUT/VIN. The inner FETs (QHSB and QLSB) are driven with a second complimentary signal of equal duty cycle, but phase shifted by 180°. By employing this driving scheme, there is a smooth transition around 50% duty ratio, where the VSW node moves from presenting GND and VIN/2 to presenting VIN and VIN/2.

The three-level can achieve higher efficiency which cannot be easily obtained using traditional buck converter. The high efficiency is due to reduced inductor ripple (volt-seconds), reduced switching loss, and use of a compact inductor with lower DCR. The device integrates low R_{DSON} FETs to optimize conduction loss. It also integrates control circuit to monitor CFLY stability and pre-conditioning.

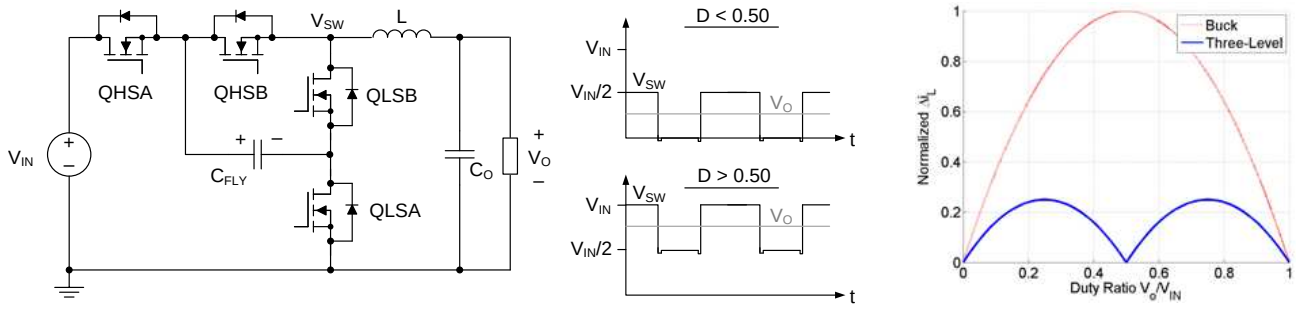

Figure 14. (a) Three-Level Buck Converter Circuit, (b) Time-Domain V_{SW} and V_O Waveforms, and (c) Inductor Current Ripple Comparison Across Duty Ratio

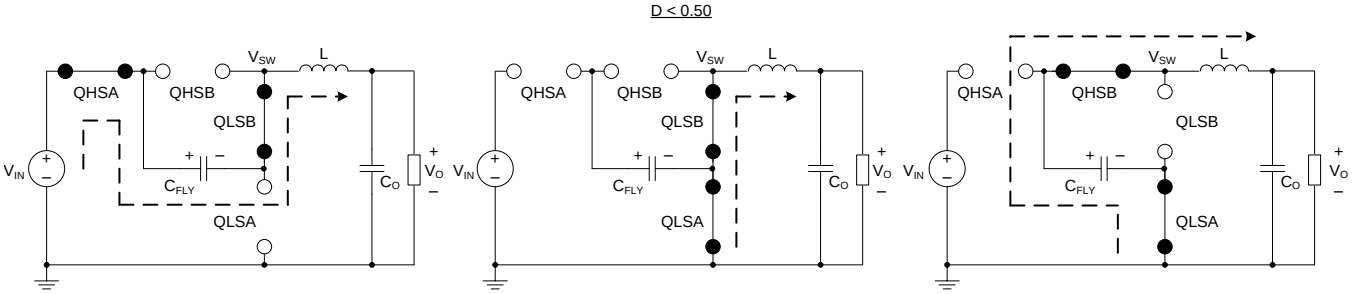

Figure 15. Three-Level Buck Converter States for Duty Ratios < 0.50

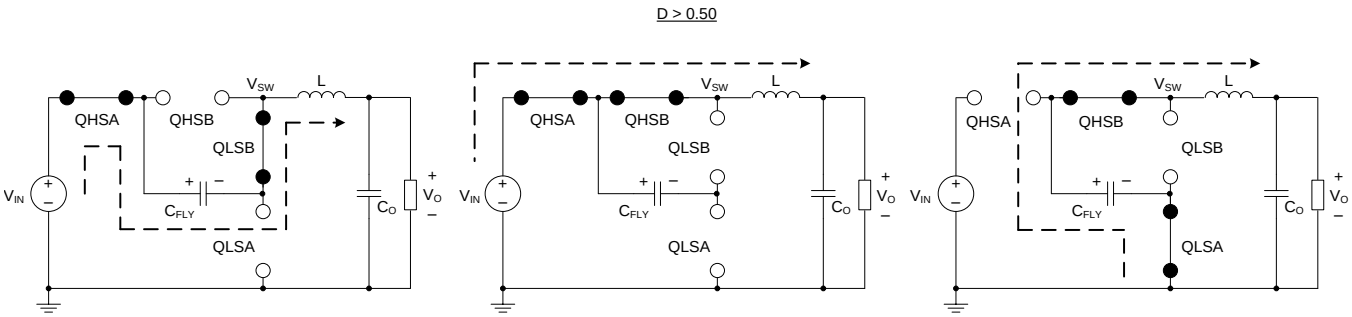

Figure 16. Three-Level Buck Converter States for Duty Ratios > 0.50

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Feature Description (continued)

7.3.8 Host Mode and Default Mode

7.3.8.1 Host Mode and Default Mode in bq25910

The bq25910 is a host controlled charger, and will automatically shut off when the I^2C watchdog timer is not reset within the timer period. In default (HIZ) mode, the device automatically disables charging until the host writes the EN_CHG bit high again and resets the watchdog timer via the WD_RST bit. When the charger is in default mode, WD_STAT bit is HIGH. When the charger is in host mode, WD_STAT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired. All the registers are in the default settings. In default mode, the device remains in HIZ mode and will not charge the battery.

Writing a 1 to the WD_RST bit forces the charger out of default mode and into host mode. All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WD_STAT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

When the watchdog timer is expired (WD_STAT bit = 1), the device returns to default mode and registers are reset to default values except as detailed in the I^2C register section. As long as the watchdog timer is expired (WD_STAT bit = 1), the device remains in Default Mode without charging the battery, regardless of the EN_CHG bit state. In order to enable charge after watchdog expired, write WD_RST = 1, and EN_CHG = 1.

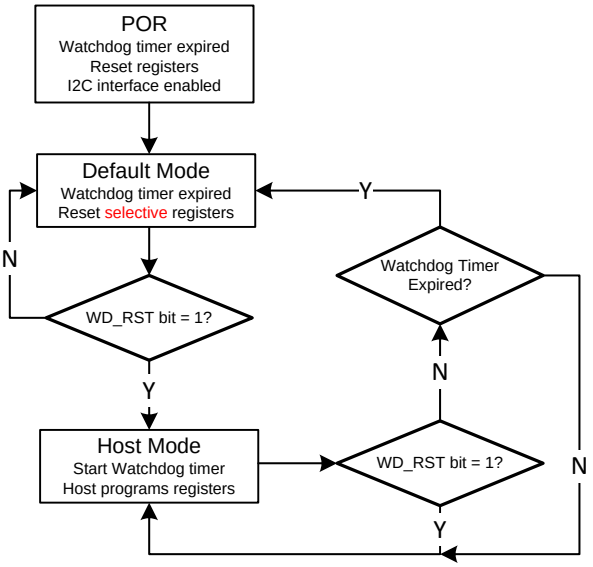

Figure 17. Watchdog Timer Flow Chart

The REG_RST bit can be used to reset all of the registers (except STATUS registers) to their default value at any time.

7.3.9 Battery Charging Management

The device charges single-cell Li-Ion battery with up to 6-A charge current for high-capacity battery.

7.3.9.1 Autonomous Charging Cycle

When battery charging is enabled (EN_CHG bit = 1) and the battery is above V_{BAT_LOWV}, the device autonomously completes a charging cycle. The device default charging parameters are listed in Table 1. The host can always control the charging operations and optimize the charging parameters by writing to the corresponding registers through I^2C.

Feature Description (continued)

Table 1. Charging Parameter Default Settings

PARAMETER	VALUE
VBAT to start fast charge (VBATLOWV)	3.5 V
Charging voltage (VREG)	4.350 V
Charging current (ICHG)	3.500 A
Termination current (ITERM)	1.000 A
Safety timer (CHG_TIMER)	12 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled by EN_CHG bit, and ICHG register is not 0 mA
- Battery voltage above V_{BAT_LOWV}
- No safety timer fault

The charger device automatically terminates the charging cycle when the charging current is below termination threshold, and device not in DPM mode or thermal regulation. Once termination is detected, an $\overline{INT}$ is asserted to the host and the EN_CHG bit gets reset to zero. After the charge is done, EN_CHG bit can initiate a new charging cycle.

Once a charging cycle is complete, an $\overline{INT}$ pulse is asserted to notify the host. In addition the status register (CHRG_STAT) indicates the different charging phases (any change in CHRG_STAT will generate an $\overline{INT}$ to notify the host):

- 000: Charging disable
- 001: Reserved
- 010: Reserved
- 011: Fast charge (constant current mode)
- 100: Taper charge (constant voltage mode)
- 101: Reserved
- 110: Reserved
- 111: Reserved

7.3.10 Master Charger and Parallel Charger Interactions

A master charger is required in the system to manage pre-charging and full termination of the battery. The bq25910 monitors the battery voltage and compares it to V_{BAT_LOWV} to ensure battery can safely take fast-charge current. Once the bq25910 turns on and begins fast-charging, the host has two options: disable (HIZ) the master charger, or continue running the master charger along with the parallel charger.

For the first option, once battery voltage reaches V_{BAT_LOWV}, the master charger maintains the BATFET on to supply system from battery (EN_HIZ = 1 on master charger), and the bq25910 provides both the charge current and system current if required. It is recommended to select V_{BAT_LOWV} equal to minimum system voltage in order to maintain system operation during transition. The bq25910 will then fast-charge the battery up to VREG and continue to regulate voltage while battery current tapers down. After the bq25910 detects termination, the host can re-enable the master charger to regulate battery voltage in CV mode down to lower termination currents.

The second mode of operation requires both chargers to stay on. In order to maximize efficiency, it is recommended to run the master charger at lower charge current than the bq25910. For example, the master charger might be set at 1 A and the bq25910 at 3.5 A to achieve total charge current of 4.5 A. In this mode of operation, the master charger provides mostly system current, while the bq25910 provides mostly charge current. In this mode of operation, the bq25910 can select V_{BAT_LOWV} as low as the battery dictates for fast-charge, since the master charger can maintain system voltage regulation and ensure system continues to operate through the transition. After the bq25910 detects termination, the master charger automatically continues to regulate battery voltage in CV mode down to lower termination current.

Figure 18 shows both options with charge current for each device as well as battery voltage.

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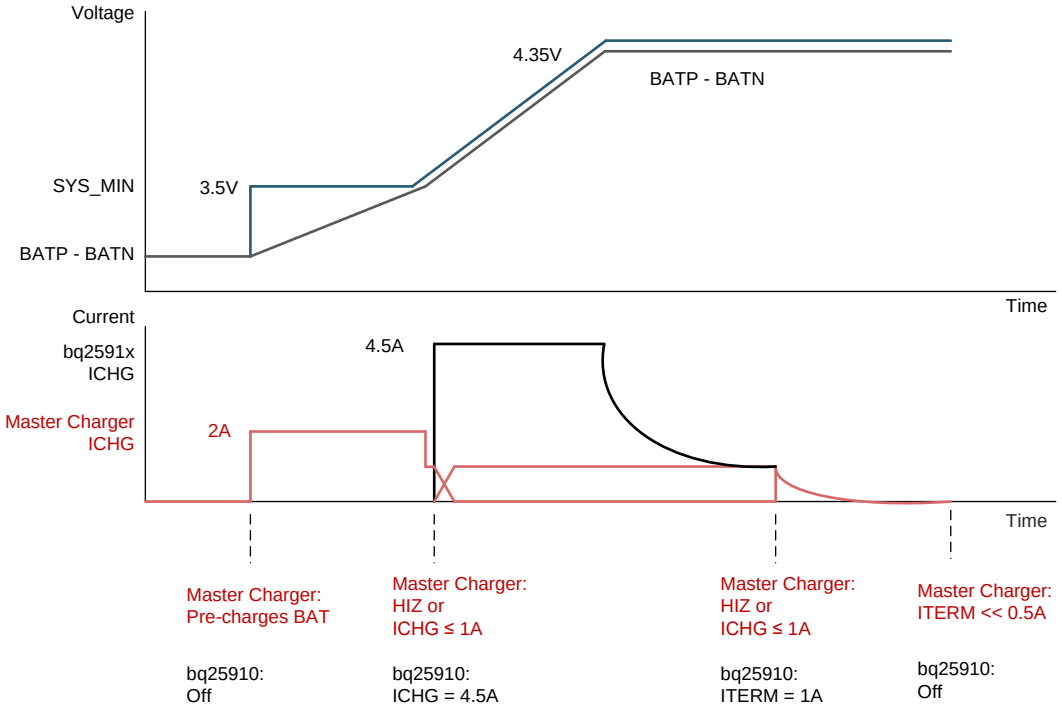

Figure 18. Master Charger and bq25910 Handoff

7.3.11 Battery Charging Profile

The device charges the battery in two phases: constant current, and constant voltage. At the beginning of a charging cycle, the device checks the battery voltage and regulates current / voltage as needed. If the battery voltage is below V_{BAT_LOWV}, it is the master charger responsibility to increase VBAT up to V_{BAT_LOWV} so the parallel charger can initiate fast charging. As BAT increases to V_{BAT_LOWV}, the master charger can stay in HIZ and the bq25910 can start fast-charging the battery with up-to 6-A ICHG. Alternatively, the master charger can remain on to maintain the system load from adapter, while the bq25910 charges the battery. The default charging settings can be found in Table 2.

Table 2. Battery Charger Setting

VBAT	CHARGING CURRENT	REG DEFAULT SETTING	CHRG_STAT
< 2 V	Master controlled (IBATSHORT)	bq25910 off	000
2 V – V_{BAT_LOWV}	Master controlled (IPRECHG)	bq25910 off	000
> V_{BAT_LOWV}	ICHG	3.500 A	011
VREG	TAPER down to ITERM	4.350 V	100

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If the charger device is in DPM regulation or thermal regulation during charging, the charging current can be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate.

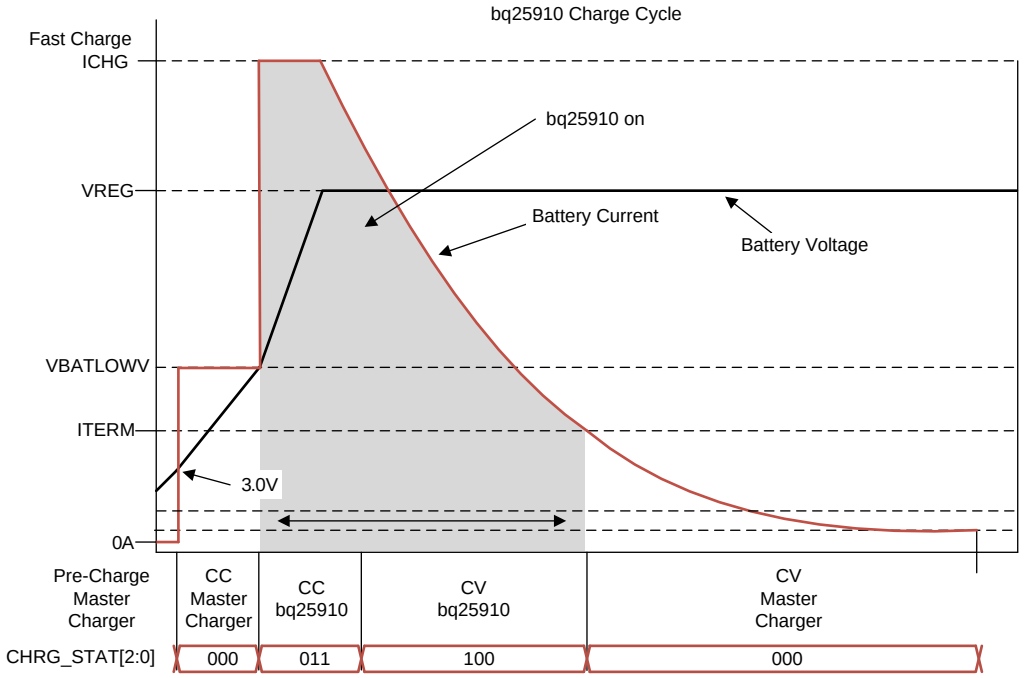

Figure 19. Battery Charging Profile Highlighting Parallel Charger Region of Operation

After the device signals charge termination done (CHRG_TERM_FLAG = 1), the master charger may choose to continue charging in CV mode or finish the charging cycle completely. The bq25910 will not start a re-charge cycle automatically, and a toggle on EN_CHG bit is required to restart a charge cycle.

7.3.11.1 Charging Termination

The device terminates a charge cycle when the battery voltage is at VREG, and the current is below termination current (ITERM). After the charging cycle is completed, the converter turns off and enters HIZ mode. At this point, the master charger can continue charging the battery down to a lower termination current, or just provide the system load from the adapter through its buck converter.

When termination occurs, the status register CHRG_STAT is set to 000, the CHRG_TERM_FLAG is set to 1, and an $\overline{\text{INT}}$ pulse is asserted to the host. The CHRG_TERM_FLAG should be used to determine if termination was detected. Termination is temporarily disabled when the charger device is in input current, input voltage or thermal regulation.

Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination. In this case, the device will continue regulating the battery voltage to VREG value until the safety timer runs out or until the EN_CHG bit is cleared.

7.3.11.2 Differential Battery Voltage Remote Sensing

For high current charging systems, resistance between the charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early, thereby increasing charge time. To speed up the charging cycle, the device provides differential remote sensing terminals for battery positive and negative terminals, which can extend the constant current charge time to deliver maximum power to the battery.

The device regulates BATP – BATN = V_{BAT} to the programmed VREG voltage. By connecting the sense terminals as close the battery as possible, the charger can deliver maximum charging power to battery. The kelvin connections to the battery can be made via a 100-Ω resistor.

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7.3.11.3 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The user can program fast charge safety timer through I^2C (CHG_TIMER bits). When safety timer expires, the TMR_FLAG bit is set to 1, and an $\overline{INT}$ pulse is asserted to the host. The safety timer feature can be disabled via I^2C using EN_TIMER bit.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the register setting. For example, if the charger is in input current regulation (IINDPM_STAT = 1) throughout the whole charging cycle, and the safety timer is set to 5 hours, then the timer will expire in 10 hours. This half clock rate feature can be disabled by setting TMR2X_EN = 0. Changing the TMR2X_EN bit while the device is running has no effect on the safety timer count, other than forcing the timer to count at half the rate under the conditions dictated above.

7.4 Device Functional Modes

7.4.1 Lossless Current Sensing

In high current charging systems, extra resistance between the charger output and the battery contribute to power loss and temperature rise. The bq25910 regulates the output current without the need of a sense resistor, thereby reducing system power loss and operating temperature. Switching FET current information is used in conjunction to inductor DCR sensing to regulate output current accurately. For optimal operation, the voltage drop across the DCR should be below 180 mV. For example, to achieve 6-A charging, the DCR should be below 30 mΩ. In addition to lossless current regulation, the switching FET current is monitored on a cycle-by-cycle basis to ensure safe operation.

7.4.2 Dynamic Power Management

To meet maximum current limit in USB spec and avoid over-loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is over-loaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit and the input voltage rises above the input voltage limit.

During DPM mode, the status register bits VINDPM_STAT (VINDPM) and/or IINDPM_STAT (IINDPM) is/are set to 1. Figure 20 shows the IINDPM response with 9-V/1.33-A (12-W) adapter, 4.0-V battery, 3.5-A charge current, and bq25910 in CV mode.

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Device Functional Modes (continued)

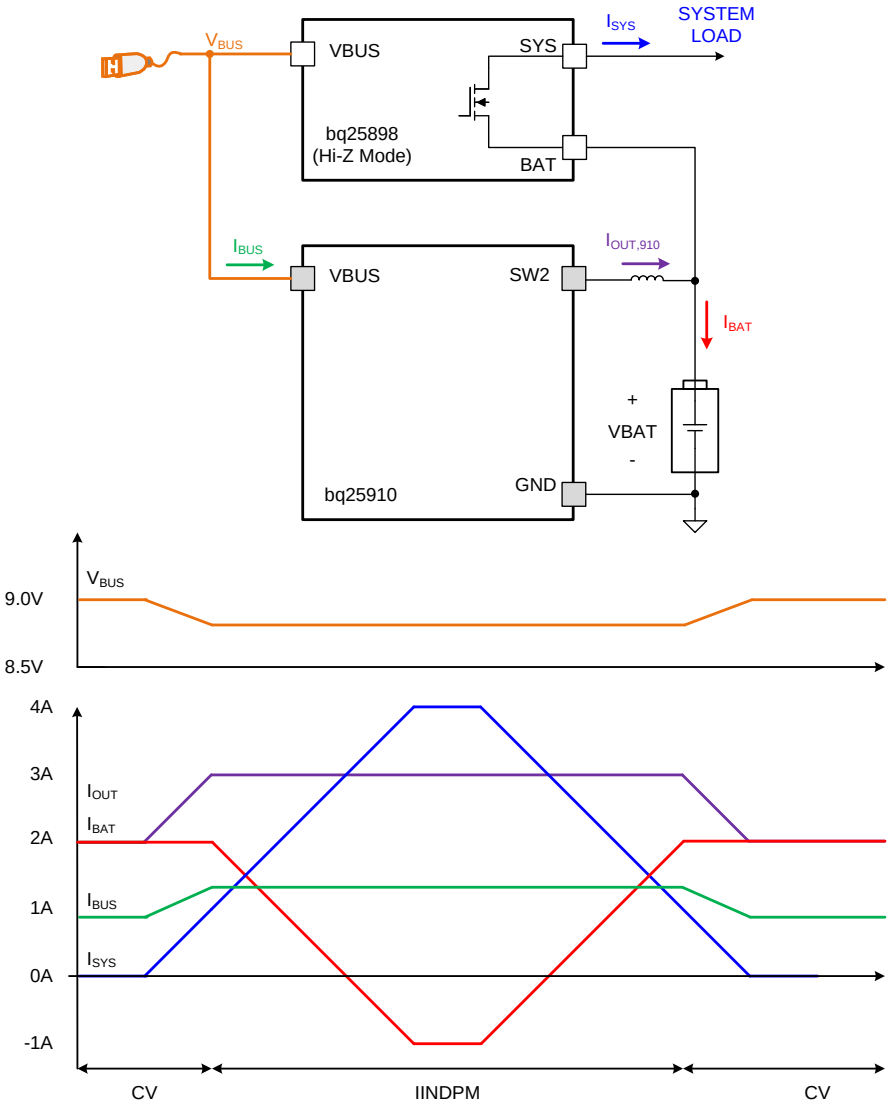

Figure 20. DPM Response

7.4.3 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor the charger operation. The $\overline{INT}$ pin notifies the system host on the device operation. By default, the following events will generate an active-low, 256-µs $\overline{INT}$ pulse.

1. Good input source detected (three conditions below met)
   - $V_{VBUS} > V_{BAT}$ (not in sleep)
   - $V_{VBUS} < V_{VBUS\_OV}$
   - $V_{VBUS} > V_{VPOORSRC}$ (typ 3.7 V) when $I_{POORSRC}$ (typ 20 mA) current is applied (not a poor source)
2. Good input source removed
3. POORSRC routine failed 7 consecutive times (connected adaptor was found to be a poor source)
4. Capacitor pre-charge routine failed (CFLY / CAUX failed to pre-charge)
5. Entering IINDPM regulation
6. Entering VINDPM regulation
7. Entering device Junction Temperature Regulation

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Device Functional Modes (continued)

8. I^2C Watchdog timer expired
   – At initial power-up, this $\overline{INT}$ gets asserted to signal I^2C is ready for communication
9. Charger changes state (CHRG_STAT value change)
10. VBUS over-voltage detected
11. Junction temperature shutdown (TSHUT)
12. Battery over-voltage detected (BATOVP)
13. CFLY fault detected
14. Charge Safety Timer Expired

Each one of these $\overline{INT}$ sources can be masked off to prevent $\overline{INT}$ pulses from being sent out when they occur. Three bits exist for each one of these events:

- The STAT bit holds the current status of each $\overline{INT}$ source
- The FLAG bit holds information on which source produced an $\overline{INT}$, regardless of current status.
- The MASK bit is used to prevent the device from sending out $\overline{INT}$ for each particular event.

When one of the above conditions occurs, the device sends out an $\overline{INT}$ pulse and keeps track of which source generated the $\overline{INT}$ via the FLAG registers. The FLAG register bits are automatically reset to zero after the host reads them, and a new edge on STAT bit is required to re-assert the FLAG.

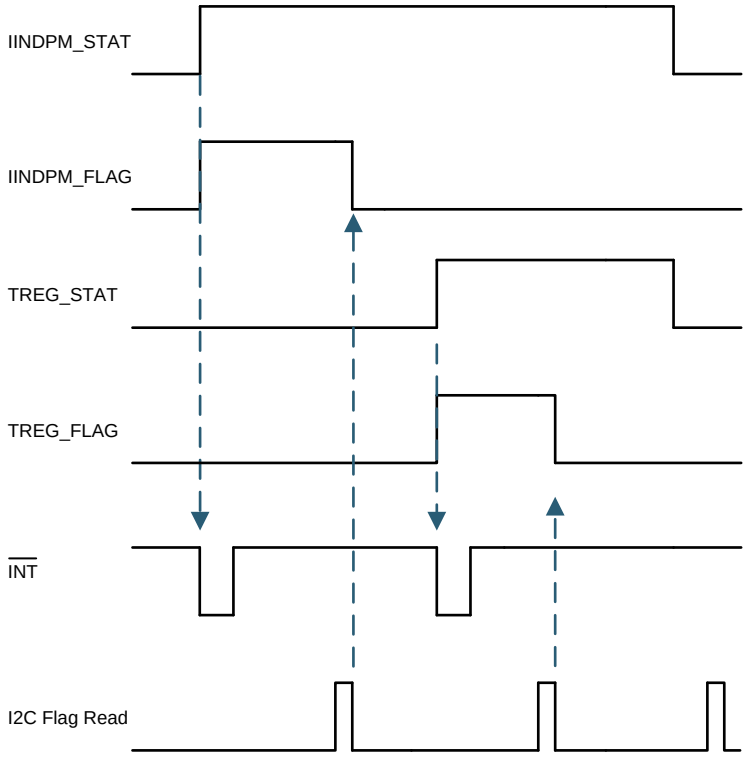

Figure 21. $\overline{INT}$ Generation Behavior Example

7.4.4 Protections

7.4.4.1 Voltage and Current Monitoring

The device closely monitors the input and output voltage, as well as switching FET currents for safe buck mode operation.

Device Functional Modes (continued)

7.4.4.1.1 Input Over-Voltage (V_{VBUS_OV})

The valid input voltage range for buck mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{VBUS_OV}, the device stops switching immediately to protect the power FETs. During input over-voltage, an INT pulse is asserted to signal the host, and the VBUS_OVP_STAT and VBUS_OVP_FLAG fault register bits get set. The device automatically starts switching again when the over-voltage condition goes away.

7.4.4.1.2 Input Under-Voltage ($V_{POORSRC}$)

The valid input voltage range for buck mode operation is V_{VBUS_OP}. If VBUS voltage falls below $V_{POORSRC}$, the device stops switching. During input under-voltage, an INT pulse is asserted to signal the host, and the PG_STAT bit gets cleared. The PG_FLAG bit will get set to signal this event. The device automatically attempts to restart switching when the under-voltage condition goes away.

7.4.4.1.3 Flying Capacitor Over- or Under-Voltage Protection (V_{CFLY_OVP} and V_{CFLY_UVP})

Under normal operating conditions the flying capacitor is balanced by the converter. However, during line transients or other failures, capacitor mis-balance is possible. The device constantly monitors the flying capacitor voltage. If VCFLY exceeds the protection limits, the device stops switching immediately. When this fault is detected, an INT pulse is asserted to notify the host, and the CFLY_STAT and CFLY_FLAG fault register bits get set. The device automatically attempts to re-balance the cap and resumes charging if successful. If the device fails to re-balance CFLY, the CAP_COND_STAT and CAP_COND_FLAG fault register bits get set, and an EN_CHG toggle is required to re-attempt charging.

7.4.4.1.4 Over Current Protection

The device monitors the outer switching FET current on a cycle-by-cycle basis . If an over-current is detected, the device responds by forcing the switching FETs to immediately discharge the inductor current and attempt current ramp-up once again.

7.4.4.2 Thermal Regulation and Thermal Shutdown

The device monitors internal junction temperature T_J to avoid overheating the chip and limits the device surface temperature in buck mode. When the internal junction temperature exceeds the preset thermal regulation limit (TREG bits), the device reduces charge current. A wide thermal regulation range from 60°C to 120°C allows the user to optimize the system thermal performance.

During thermal regulation, the actual charging current is usually below the programmed value in ICHG registers. Therefore, termination is disabled, the safety timer runs at half the clock rate, the status register TREG_STAT bit goes high, and an INT is asserted to the host.

Additionally, the device has thermal shutdown to turn off the converter when device surface temperature exceeds T_{SHUT}. The fault register TSHUT_STAT is set and an INT pulse is asserted to the host. The converter turns back on when device temperature is below T_{SHUT_HYS}.

7.4.4.3 Battery Protection

7.4.4.3.1 Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over-voltage occurs, the charger device immediately disables charge. The fault register BATOVP_STAT bit goes high and an INT pulse is asserted to signal the host.

7.5 Programming

7.5.1 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C is a bi-directional 2-wire serial interface. Only two open-drain bus lines are required: a serial data line (SDA), and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is a device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

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Programming (continued)

The device operates as a slave device with address 4BH, receiving control inputs from the master device like micro-controller or digital signal processor through REG00-REG0D. Register read beyond REG0D (0x0D) returns 0xFF. The I^2C interface supports both standard mode (up to 100 kbits/s), and fast mode (up to 400 kbits/s). When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain and must be connected to the positive supply voltage via a current source or pull-up resistor.

7.5.2 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on SCL line is LOW. One clock pulse is generated for each data bit transferred.

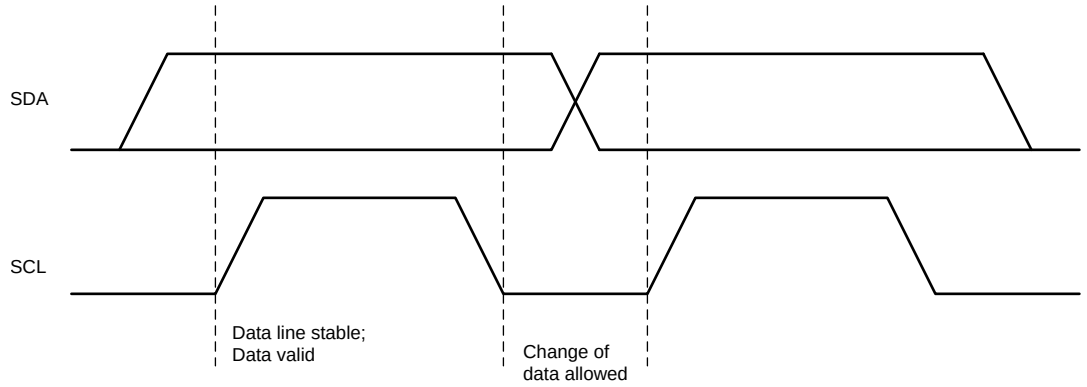

Figure 22. Bit Transfers on the I^2C Bus

7.5.3 START and STOP Conditions

All transactions begin with a START (S) and are terminated with a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

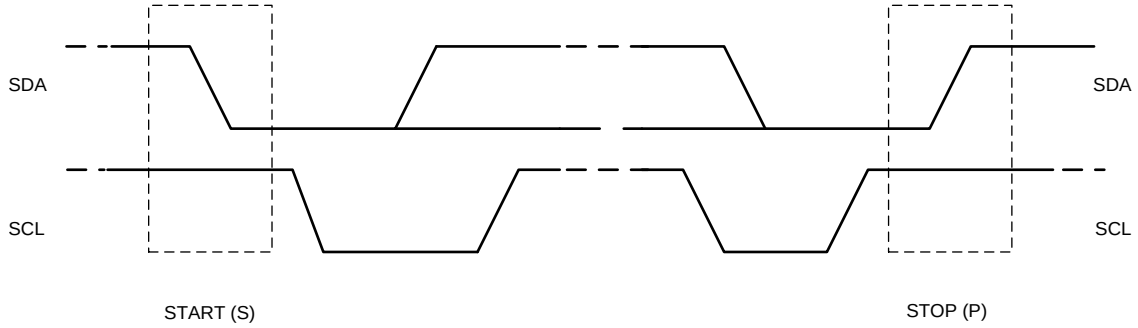

Figure 23. START and STOP Conditions on the I^2C Bus

7.5.4 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an ACKNOWLEDGE (ACK) bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the SCL line low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and releases the SCL line.

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Programming (continued)

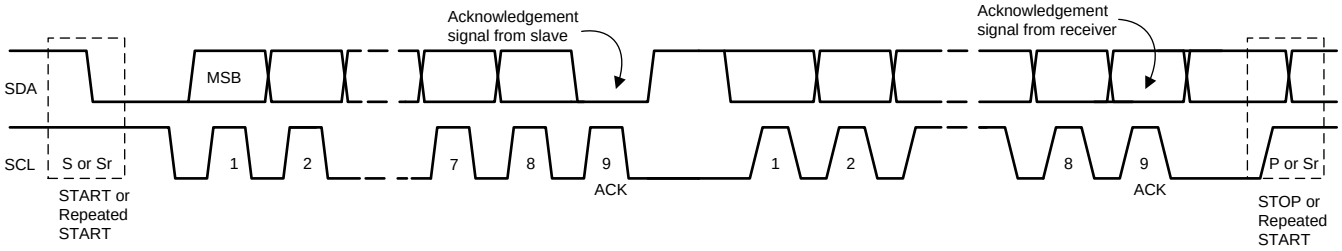

Figure 24. Data Transfer on the I²C Bus

7.5.5 Acknowledge (ACK) and Not Acknowledge (NACK)

The ACK signaling takes place after byte. The ACK bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge 9th clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this 9th clock pulse. A NACK is signaled when the SDA line remains HIGH during the 9th clock pulse. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

7.5.6 Slave Address and Data Direction Bit

After the START signal, a slave address is sent. This address is 7 bits long, followed by the 8 bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ). The device 7-bit address is defined as 1001 011' (0x4BH) by default. The address bit arrangement for 4BH is shown in Figure 25.

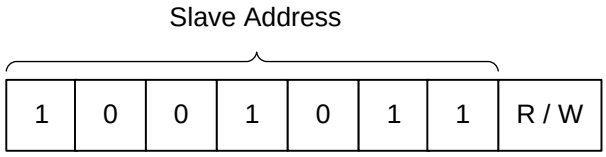

Figure 25. 14: 7-Bit Addressing (4BH)

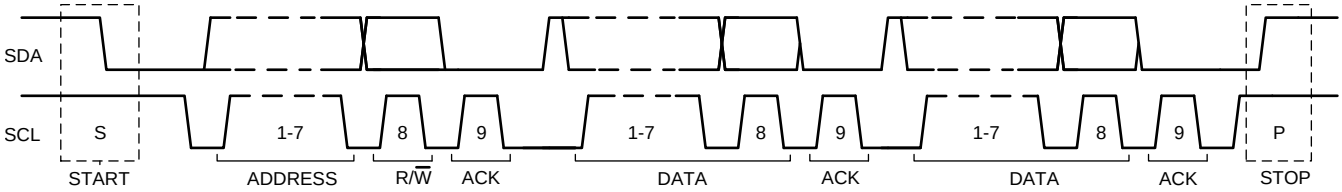

Figure 26. Complete Data Transfer on I²C Bus

7.5.7 Single Read and Write

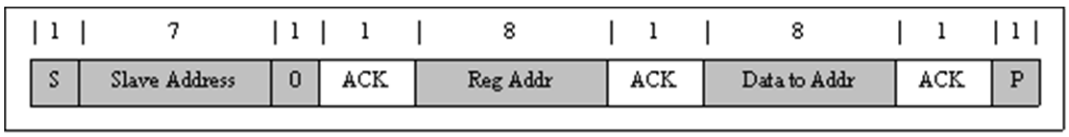

Figure 27. Single Write

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Programming (continued)

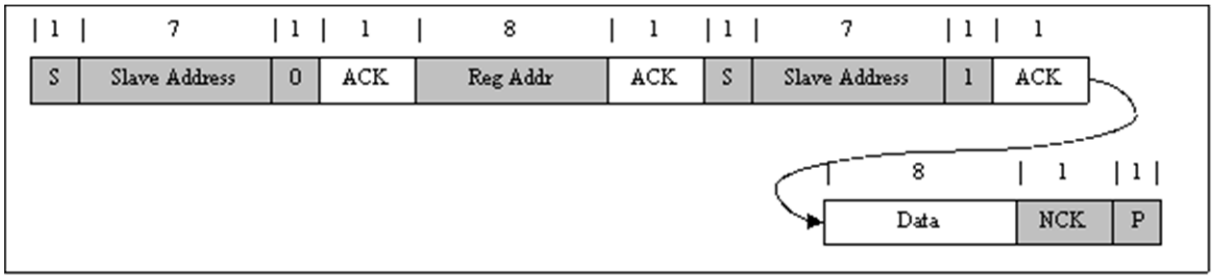

Figure 28. Single Read

If the register address is not defined, the charger device sends back NACK and returns to the idle state.

7.5.8 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write of all registers.

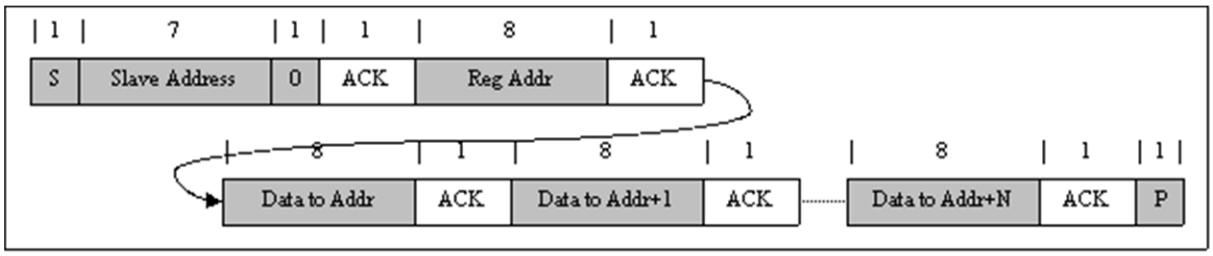

Figure 29. Multi-Write

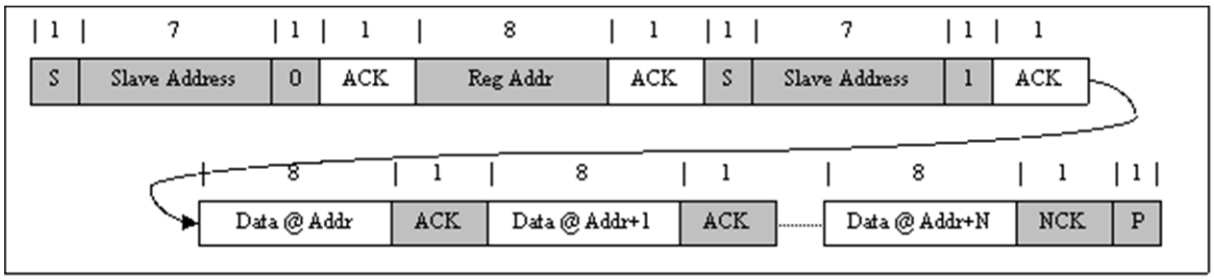

Figure 30. Multi-Read

7.6 Register Maps

7.6.1 I²C Registers

Table 3 lists the memory-mapped registers for the I²C. All register offset addresses not listed in Table 3 should be considered as reserved locations and the register contents should not be modified.

Table 3. I²C Register Summary Table

Address	Access Type	Acronym	Register Name	Section
0h	R/W	REG00	Battery Voltage Limit	Go
1h	R/W	REG01	Charge Current Limit	Go
2h	R/W	REG02	Input Voltage Limit	Go
3h	R/W	REG03	Input Current Limit	Go
4h	R/W	REG04	RESERVED	Go
5h	R/W	REG05	Charger Control 1	Go
6h	R/W	REG06	Charger Control 2	Go
7h	R	REG07	INT Status	Go
8h	R	REG08	FAULT Status	Go
9h	R	REG09	INT Flag	Go
Ah	R	REG0A	FAULT Flag	Go
Bh	R/W	REG0h	INT Mask	Go
Ch	R/W	REG0C	FAULT Mask	Go
Dh	R/W	REG0D	Part Information	Go

Complex bit access types are encoded to fit into small table cells. Table 4 shows the codes that are used for access types in this section.

Table 4. I²C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset Value		
-n		Value after reset
-X		Undefined value

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7.6.1.1 Battery Voltage Regulation Limit Register (Address = 0h) [reset = AAh]

REG00 is shown in Figure 31 and described in Table 5.

Return to Summary Table.

Figure 31. REG00 Register

7	6	5	4	3	2	1	0
VREG[7:0]							
R/W-AAh							

Table 5. REG00 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	VREG[7]	R/W	Yes	Yes	640 mV	Charge voltage limit: Offset: 3.5 V Range: 3.5 V to 4.775 V Default 4.35 V
6	VREG[6]	R/W	Yes	Yes	320 mV	
5	VREG[5]	R/W	Yes	Yes	160 mV	
4	VREG[4]	R/W	Yes	Yes	80 mV	
3	VREG[3]	R/W	Yes	Yes	40 mV	
2	VREG[2]	R/W	Yes	Yes	20 mV	
1	VREG[1]	R/W	Yes	Yes	10 mV	
0	VREG[0]	R/W	Yes	Yes	5 mV	

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7.6.1.2 Charger Current Limit Register (Address = 1h) [reset = 46h]

REG01 is shown in Figure 32 and described in Table 6.

Return to Summary Table.

Figure 32. REG01 Register

7	6	5	4	3	2	1	0
RESERVED	ICHG[6:0]						
R/W-0h	R/W-46h						

Table 6. REG01 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	RESERVED	R/W	Yes	Yes	Reserved bit always reads 0h	
6	ICHG[6]	R/W	Yes	Yes	3200 mA	Fast charge current limit Offset: 0 mA Range: 0 mA to 6000 mA Default: 3500 mA NOTE: ICHG > 6 A (78h) clamped to 6 A ICHG < 300 mA (06h) clamped to 0 A
5	ICHG[5]	R/W	Yes	Yes	1600 mA	
4	ICHG[4]	R/W	Yes	Yes	800 mA	
3	ICHG[3]	R/W	Yes	Yes	400 mA	
2	ICHG[2]	R/W	Yes	Yes	200 mA	
1	ICHG[1]	R/W	Yes	Yes	100 mA	
0	ICHG[0]	R/W	Yes	Yes	50 mA	

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7.6.1.3 Input Voltage Limit Register (Address = 2h) [reset = 04h]

REG02 is shown in Figure 33 and described in Table 7.

Return to Summary Table.

Figure 33. REG02 Register

7	6	5	4	3	2	1	0
RESERVED	VINDPM[6:0]						
R/W-0h	R/W-04h						

Table 7. REG02 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7	RESERVED	R/W	Yes	No	Reserved bit always reads 0h	
6	VINDPM[6]	R/W	Yes	No	6400 mV	Absolute input-voltage limit Offset: 3.9 V Range: 3.9 V to 14 V Default: 4.3 V NOTE: VINDPM > 14 V (65h) clamped to 14 V
5	VINDPM[5]	R/W	Yes	No	3200 mV	
4	VINDPM[4]	R/W	Yes	No	1600 mV	
3	VINDPM[3]	R/W	Yes	No	800 mV	
2	VINDPM[2]	R/W	Yes	No	400 mV	
1	VINDPM[1]	R/W	Yes	No	200 mV	
0	VINDPM[0]	R/W	Yes	No	100 mV	

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7.6.1.4 Input Current Limit Register (Address = 3h) [reset = 13h]

REG03 is shown in Figure 34 and described in Table 8.

Return to Summary Table.

Figure 34. REG03 Register

7	6	5	4	3	2	1	0
RESERVED		INDPM[5:0]					
R/W-0h		R/W-13h					

Table 8. REG03 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description	
7-6	RESERVED	R/W	Yes	No	Reserved bit always reads 0h	
5	INDPM[5]	R/W	Yes	No	3200 mA	Input current limit Offset: 500 mA Range: 500 mA to 3600 mA Default: 2400 mA NOTE: INDPM > 3600 mA (1Fh) clamped to 3600mA
4	INDPM[4]	R/W	Yes	No	1600 mA	
3	INDPM[3]	R/W	Yes	No	800 mA	
2	INDPM[2]	R/W	Yes	No	400 mA	
1	INDPM[1]	R/W	Yes	No	200 mA	
0	INDPM[0]	R/W	Yes	No	100 mA	

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7.6.1.5 Reserved Register (Address = 4h) [reset = 03h]

REG04 is shown in Figure 35 and described in Table 9.

Return to Summary Table.

Figure 35. REG04 Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-0h						R/W-3h	

Table 9. REG04 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7-0	RESERVED	R/W	Yes	Yes	Reserved bit always reads 03h

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7.6.1.6 Charger Control 1 Register (Address = 5h) [reset = 9Dh]

REG05 is shown in Figure 36 and described in Table 10.

Return to Summary Table.

When the WATCHDOG[1:0] bits change (writing the same value does not change these bits), the internal counter is reset. The same applies for the CHG_TIMER bits (changing the value in the register will reset the CHG_TIMER).

Figure 36. REG05 Register

7	6	5	4	3	2	1	0
EN_TERM	WD_RST	WATCHDOG[1:0]		EN_TIMER	CHG_TIMER[1:0]		TMR2X_EN
R/W-1h	R/W-0h	R/W-1h		R/W-1h	R/W-2h		R/W-1h

Table 10. REG05 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	EN_TERM	R/W	Yes	Yes	Termination control 0h = Disable termination 1h = Enable termination
6	WD_RST	R/W	Yes	Yes	I^2C watchdog-timer reset 0h = Normal 1h = Reset (bit returns to 0 after time reset)
5-4	WATCHDOG[1:0]	R/W	Yes	Yes	I^2C watchdog-timer settings 0h = Disable watchdog timer 1h = 40 s 2h = 80 s 3h = 160 s
3	EN_TIMER	R/W	Yes	Yes	Charging safety-timer enable 0h = Disable 1h = Enable
2-1	CHG_TIMER[1:0]	R/W	Yes	Yes	Fast-charge safety timer setting 0h = 5 hours 1h = 8 hours 2h = 12 hours 3h = 20 hours
0	TMR2X_EN	R/W	Yes	Yes	Safety timer behavior during DPM or TREG 0h = Safety timer always counts normally 1h = Safety timer count slowed by 2x during input DPM or TREG

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7.6.1.7 Charger Control 2 Register (Address = 6h) [reset = 33h]

REG06 is shown in Figure 37 and described in Table 11.

Return to Summary Table.

When the watchdog timer expires (WD_STAT = 1h), the EN_CHG bit is held in reset. To enable the charger after the watchdog expires, write a value of 1h to the WD_RST bit and a value of 1h to the EN_CHG bit.

Figure 37. REG06 Register

7	6	5	4	3	2	1	0
RESERVED		TREG[1:0]		EN_CHG	RESERVED	VBATLOWV[1:0]	
R/W-0h		R/W-3h		R/W-0h	R/W-0h	R/W-3h	

Table 11. REG06 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7-6	RESERVED	R/W	Yes	Yes	Reserved bit always reads 0h
5-4	TREG[1:0]	R/W	Yes	Yes	Thermal regulation threshold 0h = 60°C 1h = 80°C 2h = 100°C 3h = 120°C
3	EN_CHG	R/W	Yes	Yes	Charger enable configuration 0h = Charger disabled 1h = Charger enabled
2	RESERVED	R/W	Yes	Yes	Reserved bit always reads 0h
1-0	VBATLOWV[1:0]	R/W	Yes	No	V_{BAT_LOWV} threshold to start charging at ICHG programmed setting: 0h = 2.6 V 1h = 2.9 V 2h = 3.2 V 3h = 3.5 V

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7.6.1.8 INT Status Register (Address = 7h) [reset = X]

REG07 is shown in Figure 38 and described in Table 12.

Return to Summary Table.

Figure 38. REG07 Register

7	6	5	4	3	2	1	0
PG_STAT	INDPM_STAT	VINDPM_STAT	TREG_STAT	WD_STAT	CHRG_STAT[2:0]		
R-X	R-X	R-X	R-X	R-X	R-X		

Table 12. REG07 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	PG_STAT	R	Yes	Yes	Power-good status 0h = Not power good 1h = Power good
6	INDPM_STAT	R	Yes	Yes	INDPM status 0h = Normal 1h = In INDPM regulation
5	VINDPM_STAT	R	Yes	Yes	VINDPM status 0h = Normal 1h = In VINDPM regulation
4	TREG_STAT	R	Yes	Yes	Device thermal-regulation status 0h = Normal 1h = In thermal regulation
3	WD_STAT	R	Yes	No	I^2C watchdog-timer status 0h = Normal 1h = Watchdog timer expired
2-0	CHRG_STAT[2:0]	R	Yes	Yes	Charge status 0h = Not charging 1h = Reserved 2h = Reserved 3h = Fast charging (CC mode) 4h = Taper charging (CV mode) 5h = Reserved 6h = Reserved 7h = Reserved

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7.6.1.9 FAULT Status Register (Address = 8h) [reset = X]

REG08 is shown in Figure 39 and described in Table 13.

Return to Summary Table.

When the watchdog timer expires (WD_STAT = 1h), the VBUS_OVP_STAT, TSHUT_STAT, BATOVP_STAT, and CFLY_STAT bits are held in reset until the watchdog fault is cleared (WD_RST bit = 1h, or changing the WATCHDOG[1:0] bits).

Figure 39. REG08 Register

7	6	5	4	3	2	1	0
VBUS_OVP_STAT	TSHUT_STAT	BATOVP_STAT	CFLY_STAT	RESERVED	CAP_COND_STAT	POORSRC_STAT	RESERVED
R-X	R-X	R-X	R-X	R-0h	R-X	R-X	R-0h

Table 13. REG08 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	VBUS_OVP_STAT	R	Yes	Yes	Input-overvoltage status 0h = Normal 1h = Device in overvoltage protection
6	TSHUT_STAT	R	Yes	Yes	Device temperature-shutdown status 0h = Normal 1h = Device in thermal-shutdown protection
5	BATOVP_STAT	R	Yes	Yes	Battery overvoltage status 0h = Normal 1h = BATOVP (VBAT > VBATOVP)
4	CFLY_STAT	R	Yes	Yes	Flying capacitor status 0h = Normal 1h = Flying capacitor fault (VCFLY_UVP or OVP)
3	Reserved	R	Yes	Yes	Reserved bit always reads 0
2	CAP_COND_STAT	R	Yes	Yes	Capacitor precondition status 0h = Normal 1h = CFLY or CAUX precondition failed
1	POORSRC_STAT	R	Yes	Yes	Poor-source-detection status 0h = Normal 1h = POORSRC routine failed 7 consecutive times
0	RESERVED	R	Yes	Yes	Reserved bit always reads 0

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7.6.1.10 INT Flag Status Register (Address = 9h) [reset = 00h]

REG09 is shown in Figure 40 and described in Table 14.

Return to Summary Table.

All bits in REG09 are automatically cleared after a read.

Figure 40. REG09 Register

7	6	5	4	3	2	1	0
PG_FLAG	INDPM_FLAG	VINDPM_FLAG	TREG_FLAG	WD_FLAG	CHRG_TERM_FLAG	RESERVED	CHRG_FLAG
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 14. REG09 Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	PG_FLAG	R	Yes	No	Power-good INT flag 0h = Normal 1h = PG-signal toggle detected
6	INDPM_FLAG	R	Yes	No	INDPM-regulation INT flag 0h = Normal 1h = INDPM-signal rising edge detected
5	VINDPM_FLAG	R	Yes	No	VINDPM-regulation INT flag 0h = Normal 1h = VINDPM-signal rising edge detected
4	TREG_FLAG	R	Yes	No	Device temperature-regulation INT flag 0h = Normal 1h = TREG-signal rising edge detected
3	WD_FLAG	R	Yes	No	I^2C-watchdog INT flag 0h = Normal 1h = WD_STAT-signal rising edge detected
2	CHRG_TERM_FLAG	R	Yes	No	Charger-termination INT flag 0h = Normal 1h = Charger-termination signal rising edge detected
1	RESERVED	R	Yes	No	Reserved bit always reads 0
0	CHRG_FLAG	R	Yes	No	Charger status INT flag 0h = Normal 1h = CHRG_STAT[2:0] bits changed (transition to any state)

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7.6.1.11 FAULT Flag Register (Address = Ah) [reset = 00h]

REG0A is shown in Figure 41 and described in Table 15.

Return to Summary Table.

All bits in REG0A are automatically cleared after a read.

Figure 41. REG0A Register

7	6	5	4	3	2	1	0
VBUS_OVP_FLAG	TSHUT_FLAG	BATOVP_FLAG	CFLY_FLAG	TMR_FLAG	CAP_COND_FLAG	POORSRC_FLAG	RESERVED
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 15. REG0A Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	VBUS_OVP_FLAG	R	Yes	No	Input-overvoltage INT flag 0h = Normal 1h = VBUS_OVP signal rising edge detected
6	TSHUT_FLAG	R	Yes	No	Thermal-shutdown INT flag 0h = Normal 1h = TSHUT signal rising edge detected
5	BATOVP_FLAG	R	Yes	No	Battery-overvoltage INT flag 0h = Normal 1h = BATOVP signal rising edge detected
4	CFLY_FLAG	R	Yes	No	Flying capacitor fault INT flag 0h = Normal 1h = Flying capacitor fault signal rising edge detected
3	TMR_FLAG	R	Yes	No	Charger safety-timer fault INT flag 0h = Normal 1h = Charger safety-timer expired rising edge
2	CAP_COND_FLAG	R	Yes	No	Capacitor precondition fault INT flag 0h = Normal 1h = CAP_COND_STAT signal rising edge detected
1	POORSRC_FLAG	R	Yes	No	Poor-source-fault INT flag 0h = Normal 1h = POORSRC_STAT signal rising edge detected
0	RESERVED	R	Yes	No	Reserved bit always reads 0

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7.6.1.12 INT Mask Register (Address = Bh) [reset = 00h]

REG0h is shown in Figure 42 and described in Table 16.

Return to Summary Table.

Figure 42. REG0h Register

7	6	5	4	3	2	1	0
PG_MASK	INDPM_MASK	VINDPM_MASK	TREG_MASK	WD_MASK	CHRG_TERM_MASK	RESERVED	CHRG_MASK
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 16. REG0h Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	PG_MASK	R/W	Yes	No	Power-good INT mask 0h = PG toggle produces INT pulse 1h = PG toggle does not produce INT pulse
6	INDPM_MASK	R/W	Yes	No	INDPM-regulation INT mask 0h = INDPM entry produces INT pulse 1h = INDPM entry does not produce INT pulse
5	VINDPM_MASK	R/W	Yes	No	VINDPM-regulation INT mask 0h = VINDPM entry produces INT pulse 1h = VINDPM entry does not produce INT pulse
4	TREG_MASK	R/W	Yes	No	Device temperature-regulation INT mask 0h = TREG entry produces INT pulse 1h = TREG entry does not produce INT pulse
3	WD_MASK	R/W	Yes	No	I^2C watchdog-timer INT mask 0h = WD_STAT rising edge produces INT pulse 1h = WD_STAT rising edge does not produce INT pulse
2	CHRG_TERM_MASK	R/W	Yes	No	Charger-termination INT mask 0h = CHRG-termination detection produces INT pulse 1h = CHRG-termination detection does not produce INT pulse
1	RESERVED	R/W	Yes	No	Reserved bit always reads 0
0	CHRG_MASK	R/W	Yes	No	Charger-status INT mask 0h = CHRG_STAT[2:0] bit change produces INT pulse 1h = CHRG_STAT[2:0] bit change does not produce INT pulse

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7.6.1.13 FAULT Mask Register (Address = Ch) [reset = 00h]

REG0C is shown in Figure 43 and described in Table 17.

Return to Summary Table.

Figure 43. REG0C Register

7	6	5	4	3	2	1	0
VBUS_OVP_MASK	TSHUT_MASK	BATOVP_MASK	CFLY_MASK	TMR_MASK	CAP_COND_MASK	POORSRC_MASK	RESERVED
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 17. REG0C Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	VBUS_OVP_MASK	R/W	Yes	No	Input overvoltage INT mask 0h = VBUS_OVP rising edge produces INT pulse 1h = VBUS_OVP rising edge does not produce INT pulse
6	TSHUT_MASK	R/W	Yes	No	Thermal-shutdown INT mask 0h = TSHUT rising edge produces INT pulse 1h = TSHUT rising edge does not produce INT pulse
5	BATOVP_MASK	R/W	Yes	No	Battery-overvoltage INT mask 0h = BATOVP rising edge produces INT pulse 1h = BATOVP rising edge does not produce INT pulse
4	CFLY_MASK	R/W	Yes	No	Flying capacitor fault INT mask 0h = CFLY-fault rising edge produces INT pulse 1h = CFLY-fault rising edge does not produce INT pulse
3	TMR_MASK	R/W	Yes	No	Charger safety-timer fault INT mask 0h = Timer expired rising edge produces INT pulse 1h = Timer expired rising edge does not produce INT pulse
2	CAP_COND_MASK	R/W	Yes	No	Capacitor precondition-fault INT mask 0h = CAP_COND_FLAG rising edge produces INT pulse 1h = CAP_COND_FLAG rising edge does not produce INT pulse
1	POORSRC_MASK	R/W	Yes	No	Poor-source-fault INT mask 0h = POORSRC_FLAG rising edge produces INT pulse 1h = POORSRC_FLAG rising edge does not produce INT pulse
0	RESERVED	R/W	Yes	No	Reserved bit always reads 0

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7.6.1.14 Part Information Register (Address = Dh) [reset = 09h]

REG0D is shown in Figure 44 and described in Table 18.

Return to Summary Table.

Figure 44. REG0D Register

7	6	5	4	3	2	1	0
REG_RST	PN[3:0]				DEV_REV[2:0]		
R/W-0h	R-1h				R-1h		

Table 18. REG0D Register Field Descriptions

Bit	Field	Type	Reset by REG_RST	Reset by WATCHDOG	Description
7	REG_RST	R/W	No	No	Register preset 0h = Keep the current register settings 1h = Reset to default register values and reset the safety timer NOTE: This bit resets to 0 after the register reset is complete.
6-3	PN[3:0]	R	No	No	Part number 1h = bq25910
2-0	DEV_REV[2:0]	R	No	No	Device revision: 001

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application consists of the device configured as an I^2C controlled single cell, parallel battery charger for Li-Ion and Li-polymer batteries used in a wide range of smartphones and other portable devices. It integrates an input reverse-block FET (QBLK), four switching FETs for three-level operation (QHSA – QLSA), and a bootstrap cap control to drive HS gates.

8.2 Typical Application

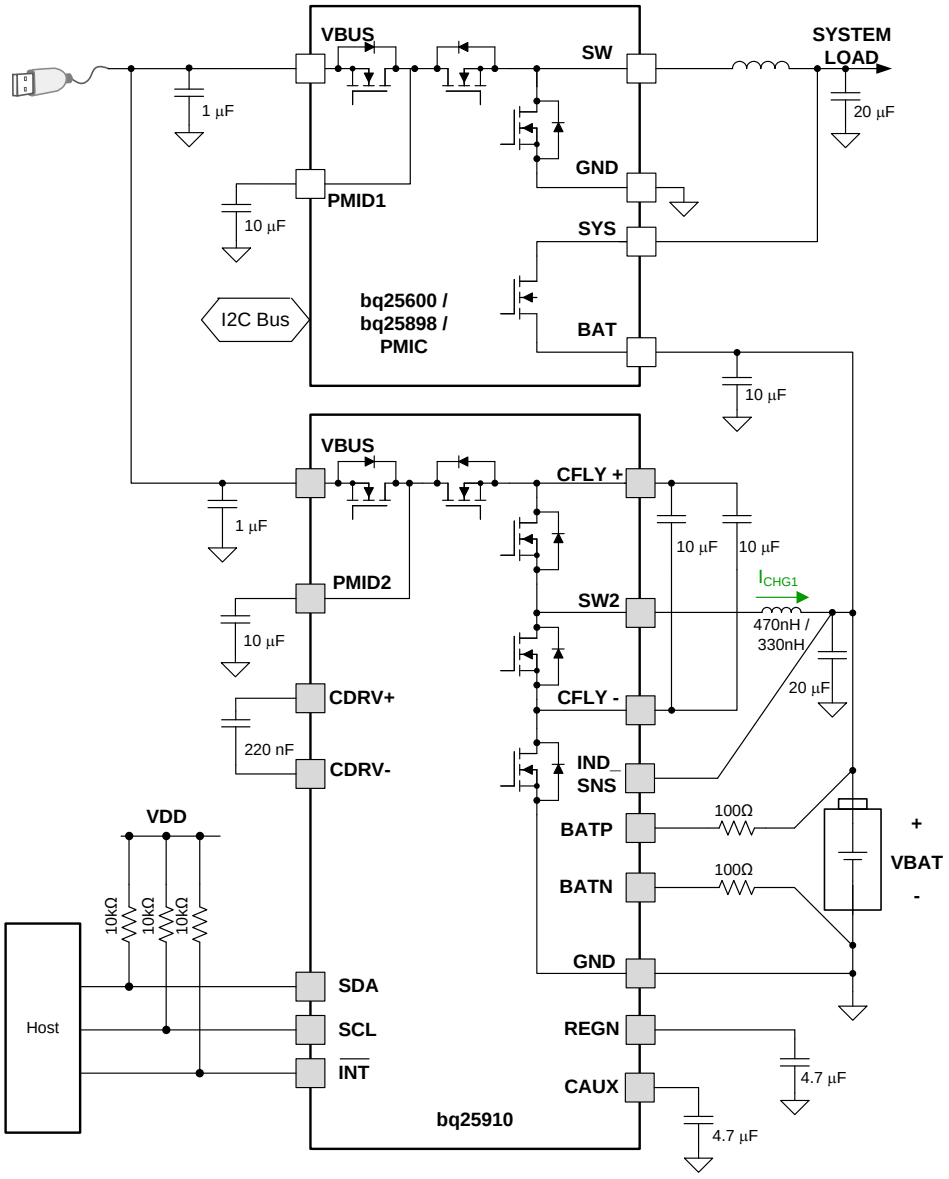

Figure 45. bq25910 Application Test Configuration

Typical Application (continued)

8.2.1 Design Requirements

For this design example, use the parameters shown in Table 19.

Table 19. Design Parameters

PARAMETER	VALUE
Input Voltage Range	3.9 V to 14 V
Input Current Limit	2.4 A
Fast Charge Current	3.5 A
Battery Regulation Voltage	4.35 V

8.2.2 Detailed Design Procedure

8.2.2.1 External Passive Recommendation

The following part numbers are recommended for correct operation of bq25910.

Table 20. Recommended External Components

PASSIVE	UP TO 9VBUS ±10%	UP TO 12VBUS ±10%
Inductor	HMLQ25201B-R33	DFE252012F-R47
	MPIM252010E-R33	DFE252010F-R47
CFLY (10 µF, X5R, 16 V)	2x GRM188R61C106MAALD	
CAUX (4.7 µF, X5R, 16 V)	1x GRM155R61A475MEAAD	

8.2.2.2 Inductor Selection

The bq25910 is a three-level converter with a fixed switching frequency of 750 kHz, allowing the use of small inductor and capacitor values. The inductor saturation current should be higher than the output current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + \frac{I_{RIPPLE}}{2} \quad (1)$$

The inductor ripple current depends on input voltage (V_{BUS}), duty cycle ($D = V_{BAT}/V_{BUS}$), switching frequency (f_{sw}) and inductance (L):

$$I_{RIPPLE} = \frac{VBUS\left(0.5 \times |D - 0.5| - (D - 0.5)^2\right)}{Lf_{sw}} \quad (2)$$

The maximum inductor ripple current happens with D = 1/3 or D = 2/3. The recommended value of inductance is 330 nH for 9-V applications or 470 nH for 12-V applications (750 kHz).

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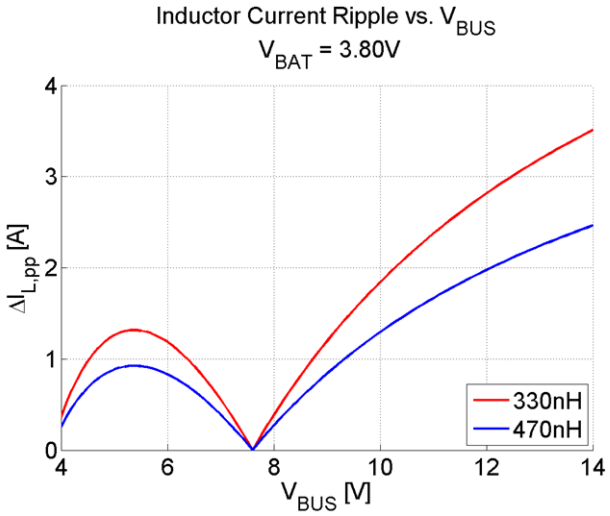

Figure 46. Inductor Current Ripple as function of V_{BUS} with Fixed V_{BAT}

Table 21. Recommended Inductor values

VBUS	INDUCTOR VALUE
3.9 V < VBUS < 10 V	330 nH
3.9 V < VBUS < 14 V	470 nH

8.2.2.3 Input Capacitor

Input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS current occurs when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated by the following equation:

$$I_{CIN} = I_{CHG}\sqrt{D(1-D)} \tag{3}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed as close as possible to PMID and GND pins. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for 12-V input voltage. 10-µF capacitance is suggested for up-to 6-A charging current.

8.2.2.4 Flying Capacitor

Flying capacitor selection must meet criteria related to current ripple and voltage ripple. Just as the input capacitor, the flying capacitor should also have enough ripple current rating to absorb the RMS current through it:

$$I_{CFLY} = \sqrt{2\left(0.5 - \left|D - 0.5\right|\right)\left(I^2_{CHG} + \frac{I^2_{RIPPLE}}{12}\right)} \tag{4}$$

This function becomes maximum when D = 0.5, because at that point the capacitor is in series with the inductor for a complete switching cycle, and their RMS currents are the same. The flying capacitor should be sized to handle the full charge current in the scenario where D = 0.5.

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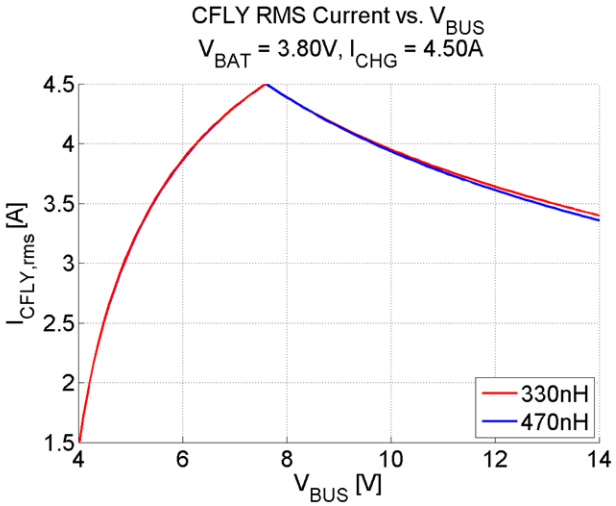

Figure 47. Flying Capacitor RMS Current vs. V_{BUS} with Fixed V_{BAT} and I_{CHG}

Additionally, the flying capacitor voltage ripple should be kept under 10% of V_{BUS}/2 to ensure loop stability. This quantity is given by the following equation:

$$\Delta V_{CFLY} = \frac{I_{CHG}\left(0.5 - \left|D - 0.5\right|\right)}{C_{FLY} f_{SW}} \quad (5)$$

It is recommended to use at least two 16-V, 10-µF, low ESR ceramic capacitors in parallel to achieve both RMS current rating and maintain voltage ripple <10% in the flying capacitor for up-to 6-A charge current application. The following curve shows what the ripple voltage of CFLY might look like for such a configuration by taking into account voltage derating of the capacitor and plugging the effective capacitance value into equation above at different charge currents and V_{BUS} voltages.

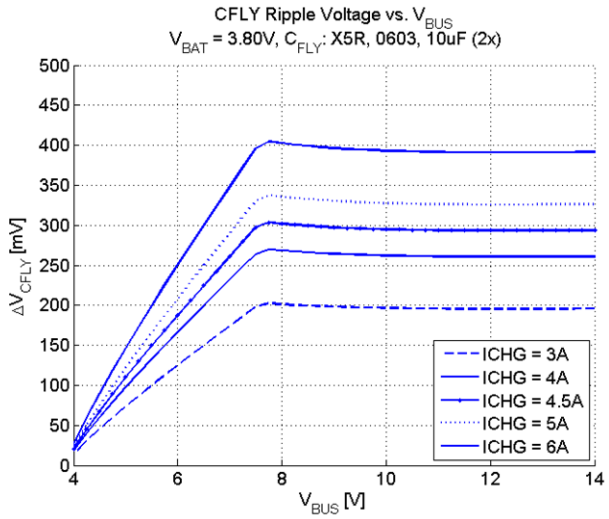

Figure 48. Flying Capacitor Ripple Voltage vs. V_{BUS} with Fixed V_{BAT}

Table 22. Recommended CFLY Values

CHARGE CURRENT	CFLY CONFIGURATION
ICHG < 3.5 A	1 x 0603 (10 µF, X5R, 16 V)
ICHG > 3.5 A	2 x 0603 (10 µF, X5R, 16 V)

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8.2.2.5 Output Capacitor

Output capacitor also should have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{COUT} = \frac{I_{RIPPLE}}{2\sqrt{3}} \approx 0.29 \times I_{RIPPLE} \quad (6)$$

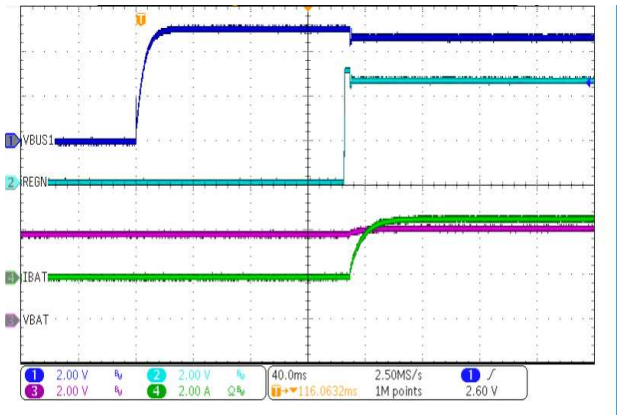
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_{SYS} = \frac{I_{RIPPLE}}{16 C_O f_{SW}} \quad (7)$$

At certain input/output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC. The preferred ceramic capacitor is 20 μF, 6.3 V or higher rating, X7R or X5R.

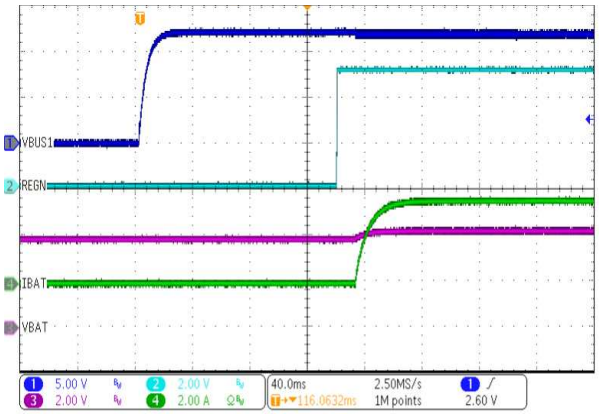
8.2.3 Application Curves

CBUS = 1 μF, CPMID = 10 μF, CBAT = 20 μF, CFLY = 20 μF, L = DFE252012F-R47 (470 nH) (unless otherwise noted)



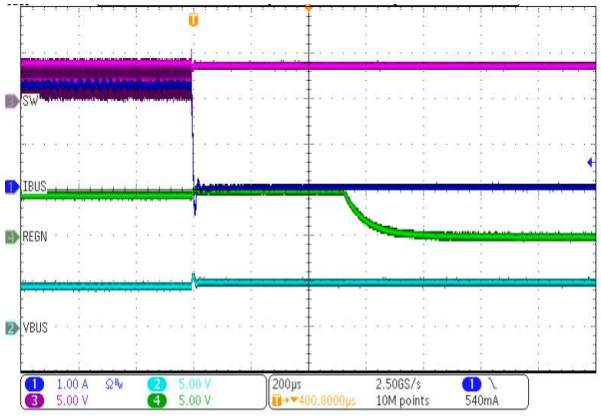
VBUS = 5 V, VBAT = 3.8 V

Figure 49. Adapter Power Up with Charge Enabled



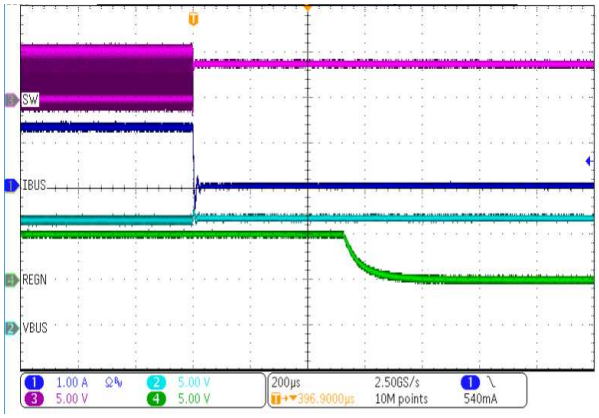
VBUS = 12 V, VBAT = 3.8 V

Figure 50. HV Adapter Power Up with Charge Enabled



VBUS = 5 V, VBAT = 3.5 V, ICHG = 3 A

Figure 51. Charge Disable



VBUS = 12 V, VBAT = 3.5 V, ICHG = 4 A

Figure 52. HV Adapter Charge Disable

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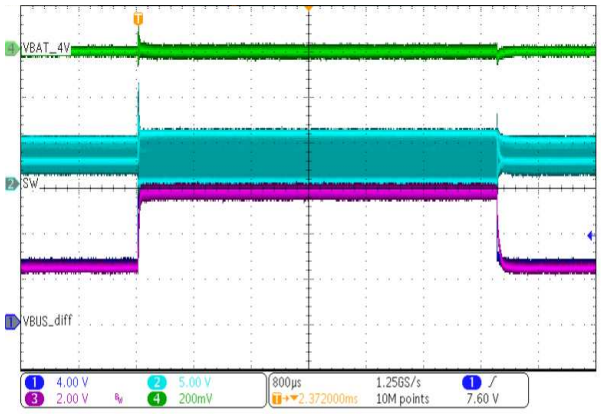
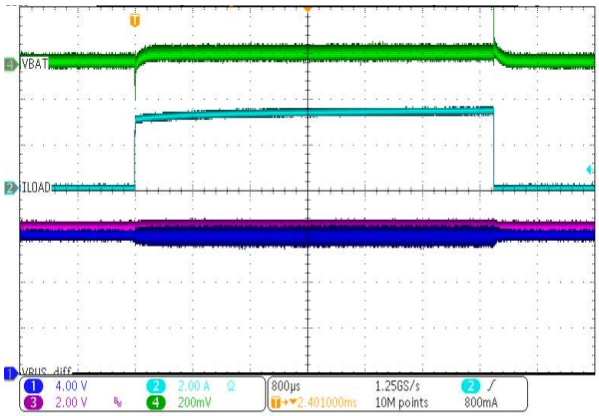
CBUS = 1 µF, CPMID = 10 µF, CBAT = 20 µF, CFLY = 20 µF, L = DFE252012F-R47 (470 nH) (unless otherwise noted)



VBUS = 5 V -> 12 V -> 5 V, VBAT = 4 V, ICHG = 1 A

CH 1 = VBUS, CH2 = SW, CH3 = CFLY differential, CH4 = VBAT

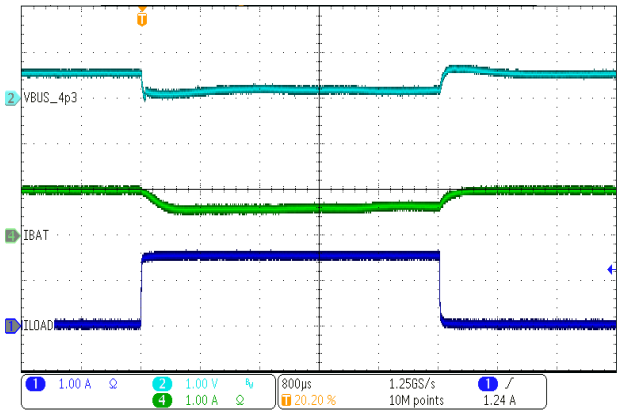
Figure 53. Line Transient Response in CC Mode



VBUS = 12 V, VBAT = 4.35 V, ICHG = 4 A, IBAT = 1 A -> 4 A -> 1 A

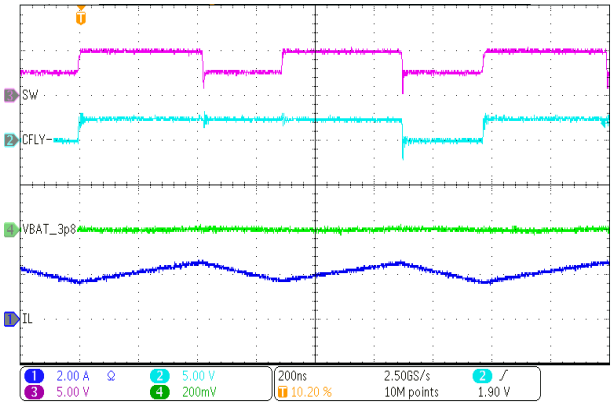
CH 1 = VBUS, CH2 = ILOAD, CH3 = CFLY differential, CH4 = VBAT

Figure 54. Load Transient Response in CV Mode



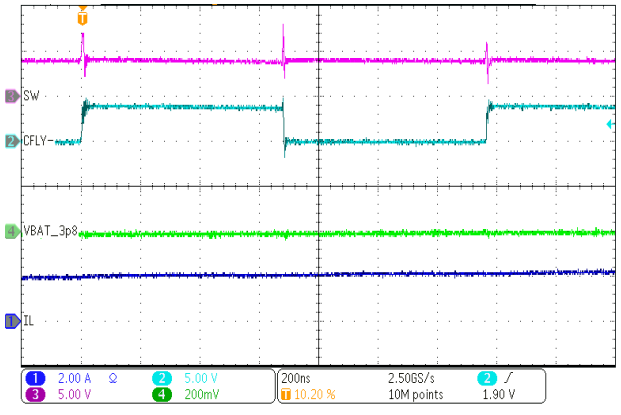
VBAT = 4.1 V, VINDPM = 4.3 V

Figure 55. VINDPM Response



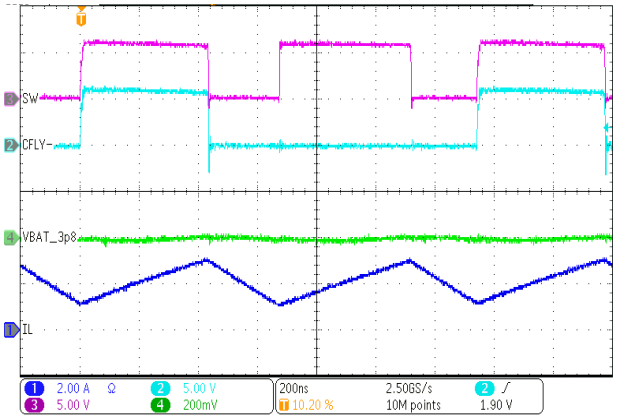
VBUS = 5 V, VBAT = 3.8 V, ICHG = 2 A, (D > 50%)

Figure 56. PWM Switching Waveform



VBUS = 8 V, VBAT = 3.8 V, ICHG = 2 A, (D approx. 50%)

Figure 57. PWM Switching Waveform



VBUS = 12 V, VBAT = 3.8 V, ICHG = 2 A (D < 50%)

Figure 58. PWM Switching Waveform

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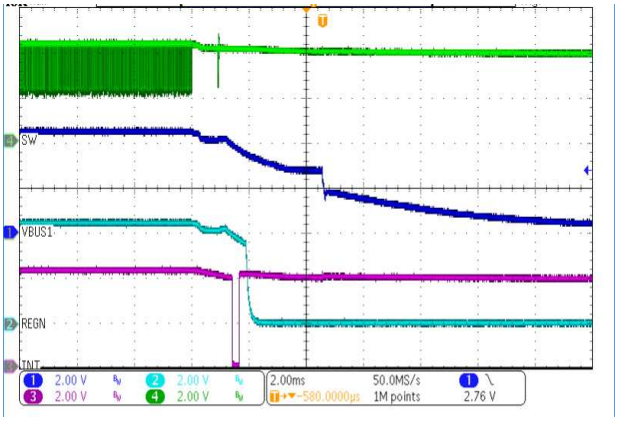
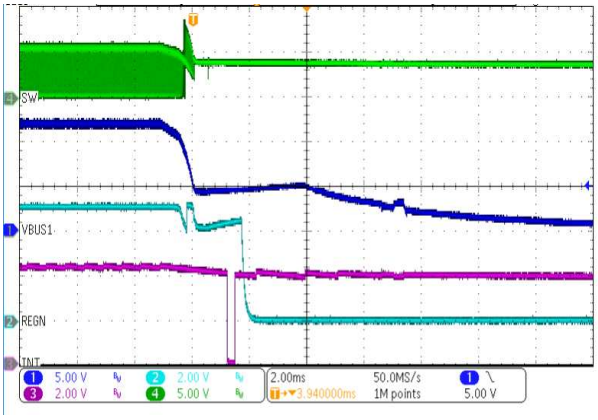
CBUS = 1 µF, CPMID = 10 µF, CBAT = 20 µF, CFLY = 20 µF, L = DFE252012F-R47 (470 nH) (unless otherwise noted)



VBUS = 5 V, VBAT = 3.8 V

Figure 59. Adapter Removal



VBUS = 12 V, VBAT = 3.8 V

Figure 60. Adapter Removal

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9 Power Supply Recommendations

In order to charge single-cell Li-Ion battery, the device requires a power supply between 3.9 V and 14 V with at least 500-mA current rating connected to VBUS. Additionally, a single-cell Li-Ion battery with voltage > V_{BAT_LOWV} should be connected between at the output of the switched inductor, between BATP and BATN terminals.

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10 Layout

10.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Utilize at least four-layer board for optimal layout, and assign one layer as solid ground plane near the IC to minimize high-frequency current path
2. Place flying capacitor as close to CLFY+ and CLFY– bumps as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection.
3. Place input capacitor as close as possible to PMID bumps and PGND bumps and use solid GND plane underneath the IC. Use plenty of vias close to PMID capacitor GND terminal and IC PGND bumps to ensure low parasitic connection to GND plane.
4. Place inductor input terminal as close to SW bumps as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current.
5. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the device ground with a short copper trace connection or GND plane.
6. Decoupling capacitors should be placed next to the device and make trace connection as short as possible.
7. Ensure that there are sufficient thermal vias directly under bumps of the power FETs, connecting to copper on other layers.
8. The via size and number should be enough for a given current path.
9. Route BATP and BATN away from switching nodes such as SW and CFLY+, CFLY–.

   Refer to the EVM design and Figure 61 for the recommended component placement with trace and via locations.

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10.2 Layout Example

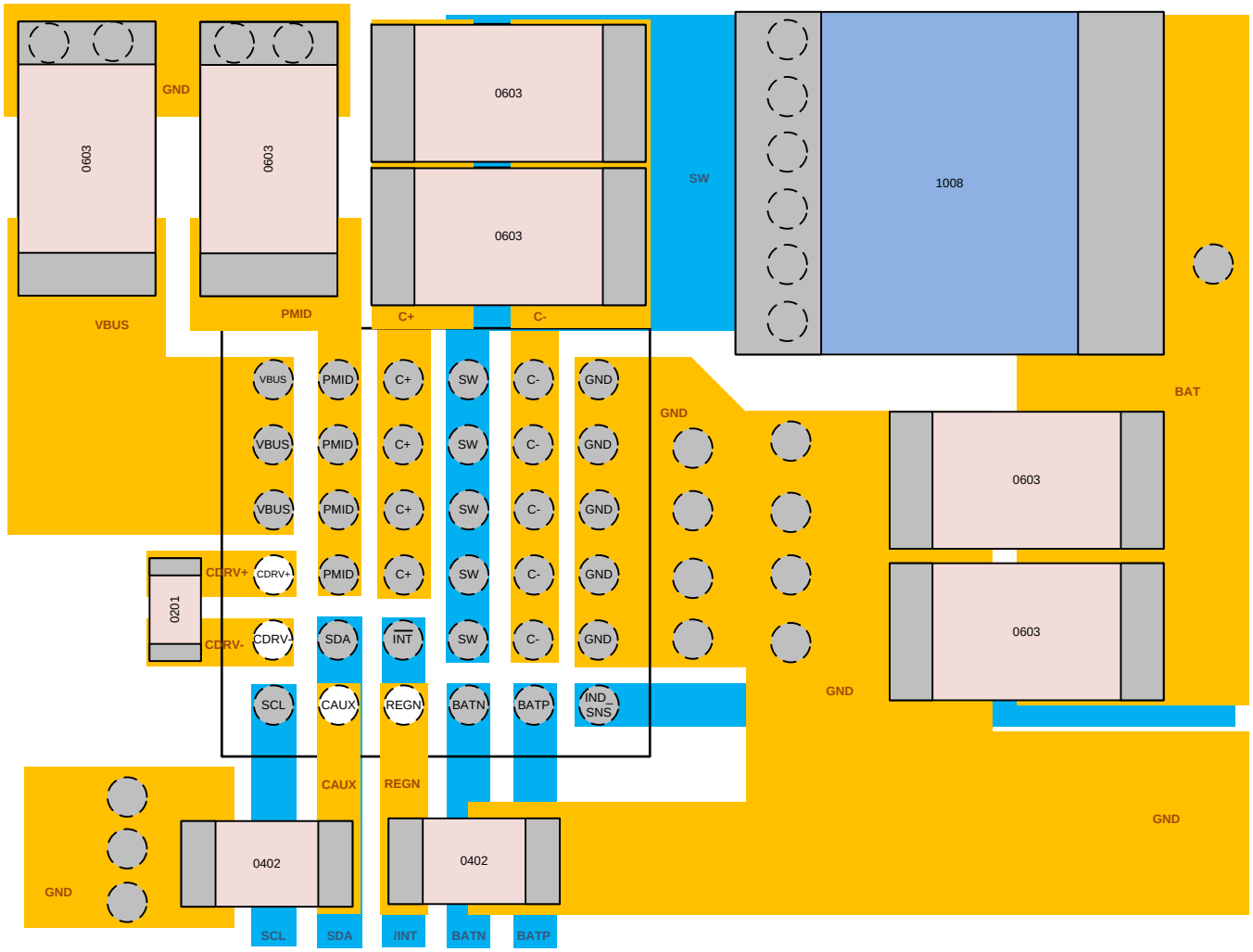

Figure 61. bq25910 PCB Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

11.1.1.1 Third-Party Products Disclaimer

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To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25910YFFR	ACTIVE	DSBGA	YFF	36	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25910	Samples
BQ25910YFFT	ACTIVE	DSBGA	YFF	36	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 85	BQ25910	Samples
PQ25910YFFT	ACTIVE	DSBGA	YFF	36	250	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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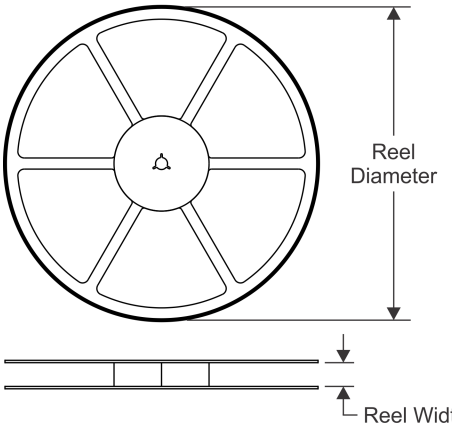
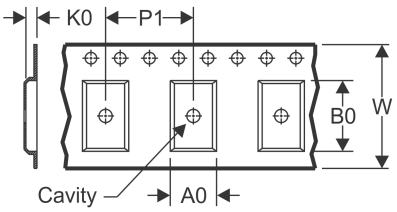
TAPE AND REEL INFORMATION

REEL DIMENSIONS

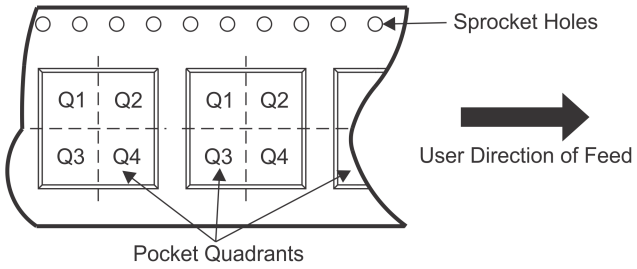


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

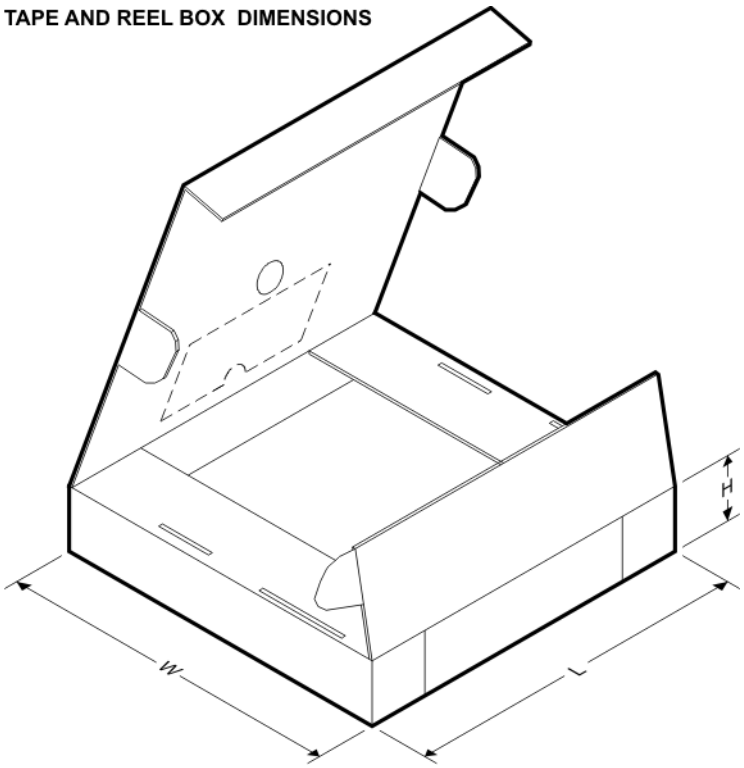
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

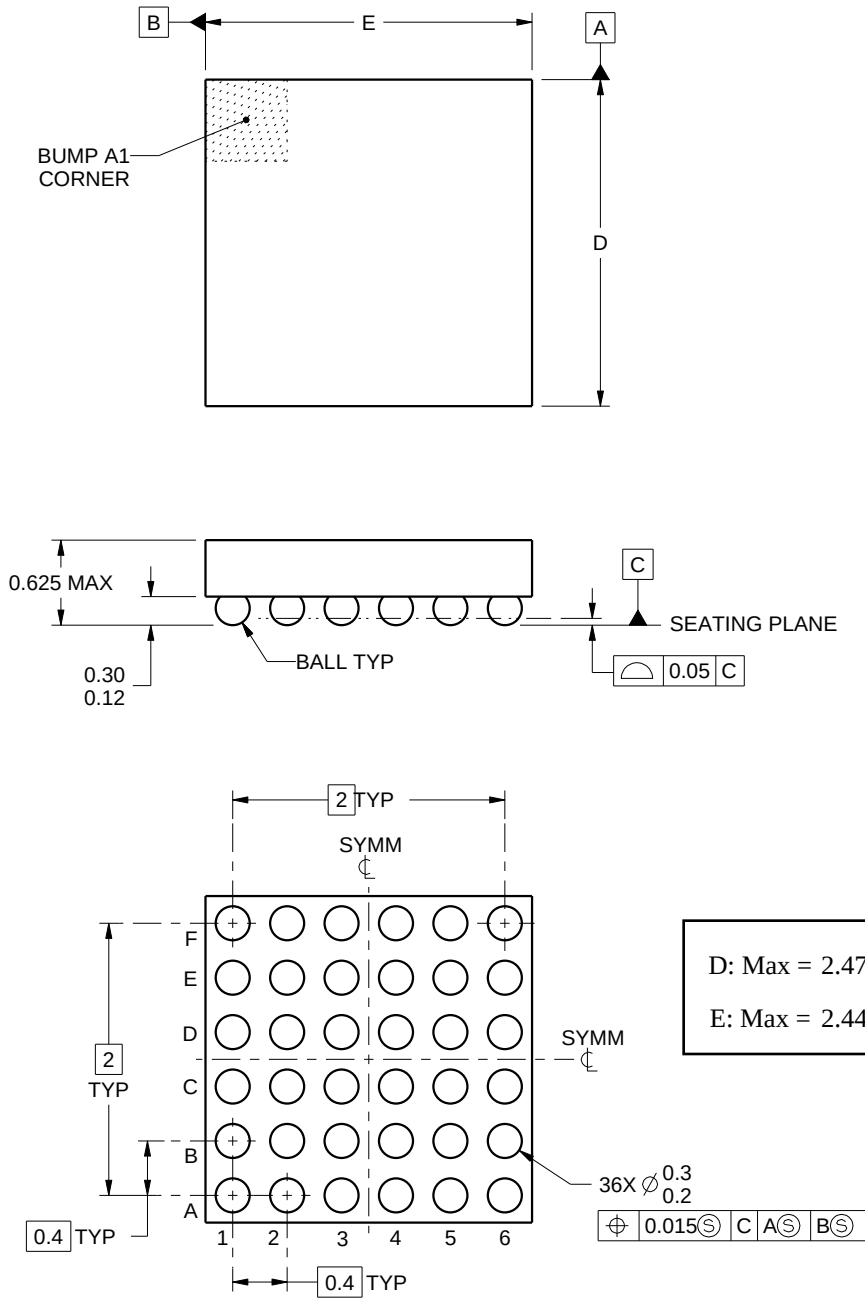
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25910YFFR	DSBGA	YFF	36	3000	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1
BQ25910YFFT	DSBGA	YFF	36	250	180.0	8.4	2.54	2.54	0.76	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25910YFFR	DSBGA	YFF	36	3000	182.0	182.0	20.0
BQ25910YFFT	DSBGA	YFF	36	250	182.0	182.0	20.0



D: Max = 2.472 mm, Min =2.412 mm

E: Max = 2.444 mm, Min =2.384 mm

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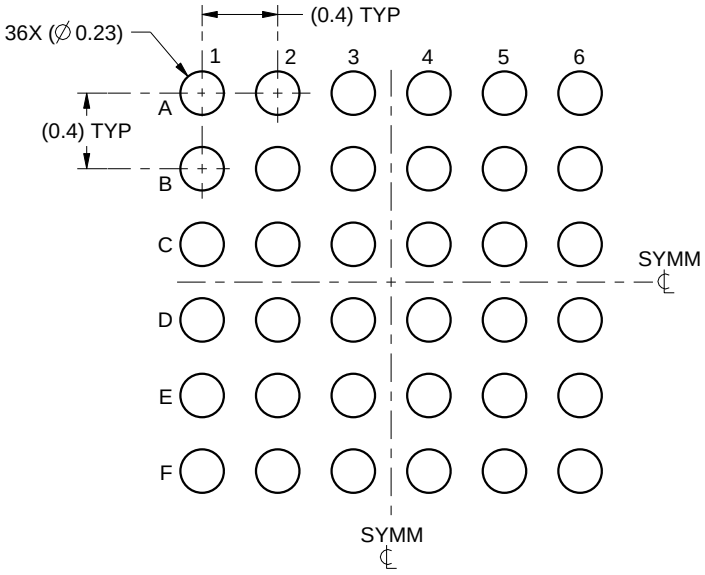
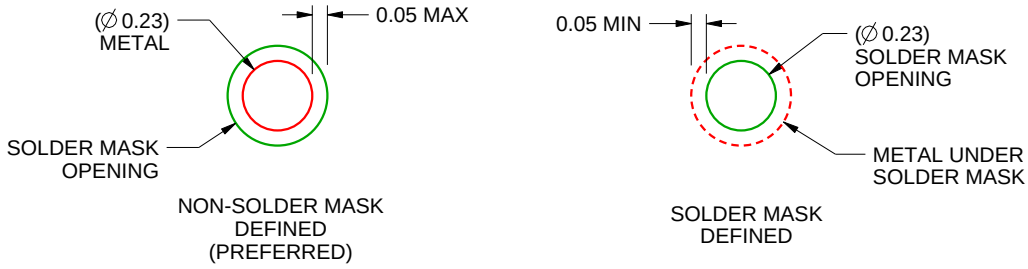
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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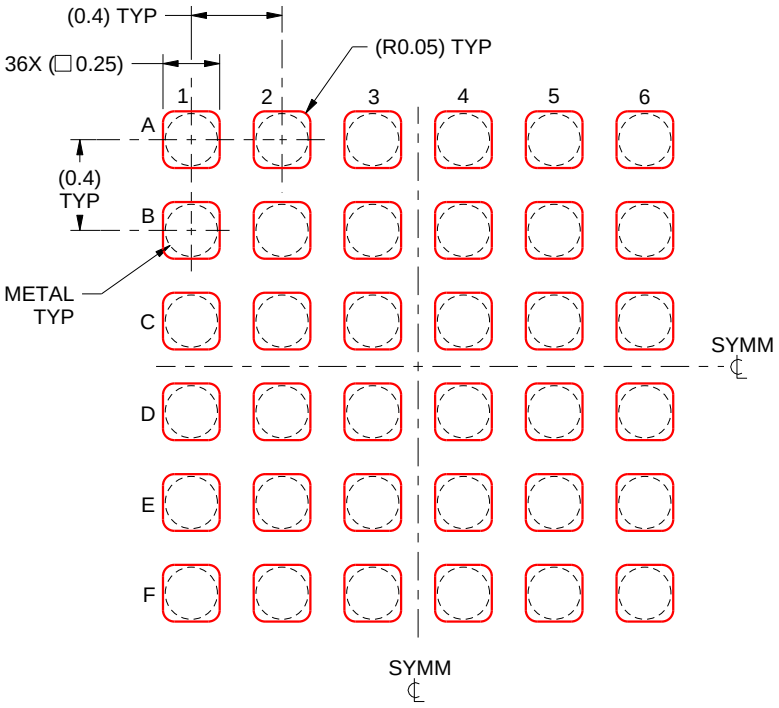
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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